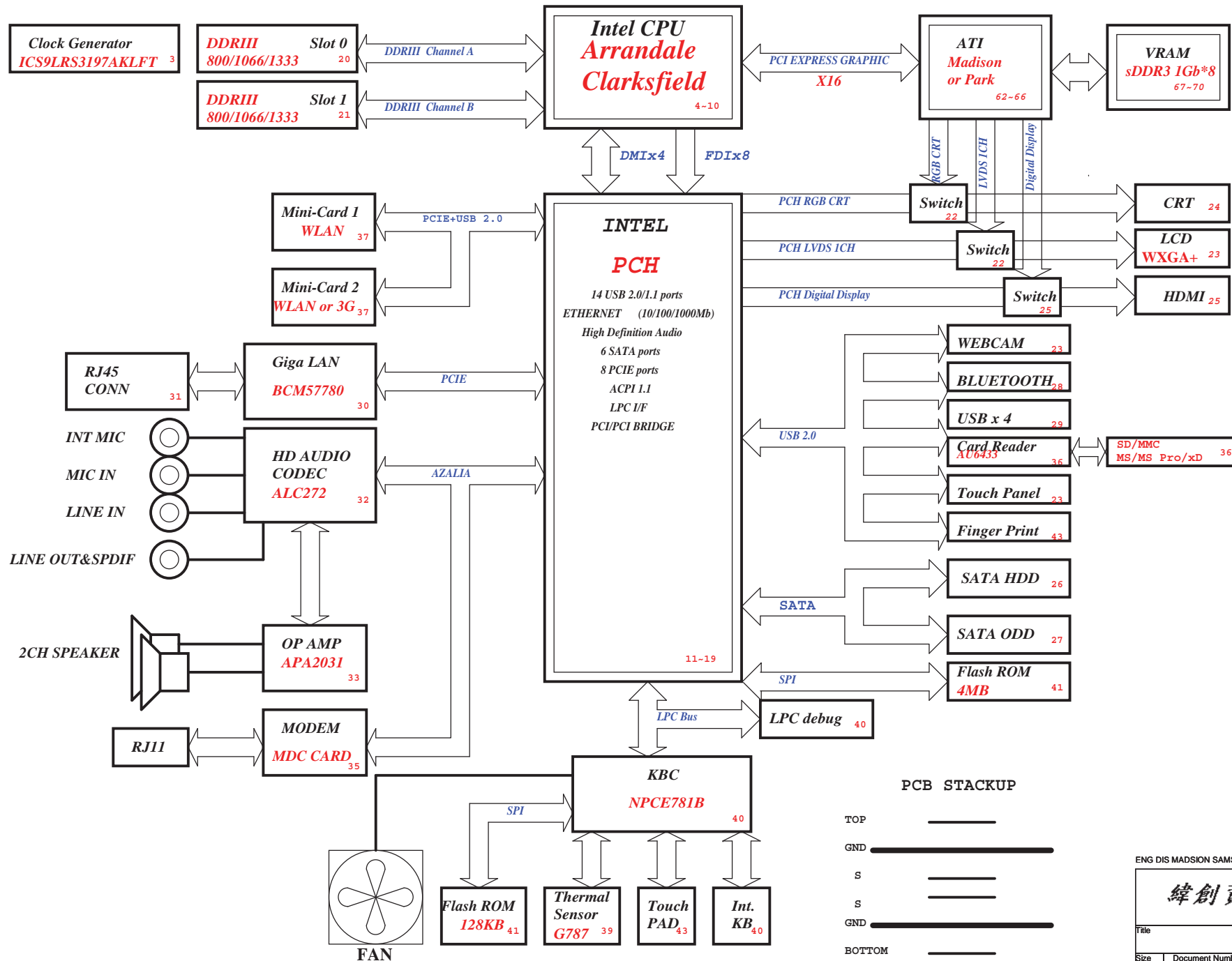


JV50-CP Block Diagram

PCB P/N : 48.4GD01.0SB

REVISION : SB 09285



CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47, 48
SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51
RT9025	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50
G2997	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 52
SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 54
SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 55

CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

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Title			
Block Diagram			
Size A3	Document Number JV50-CP		Rev SA
Date: Thursday, August 27, 2009	Sheet 1	of 57	

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

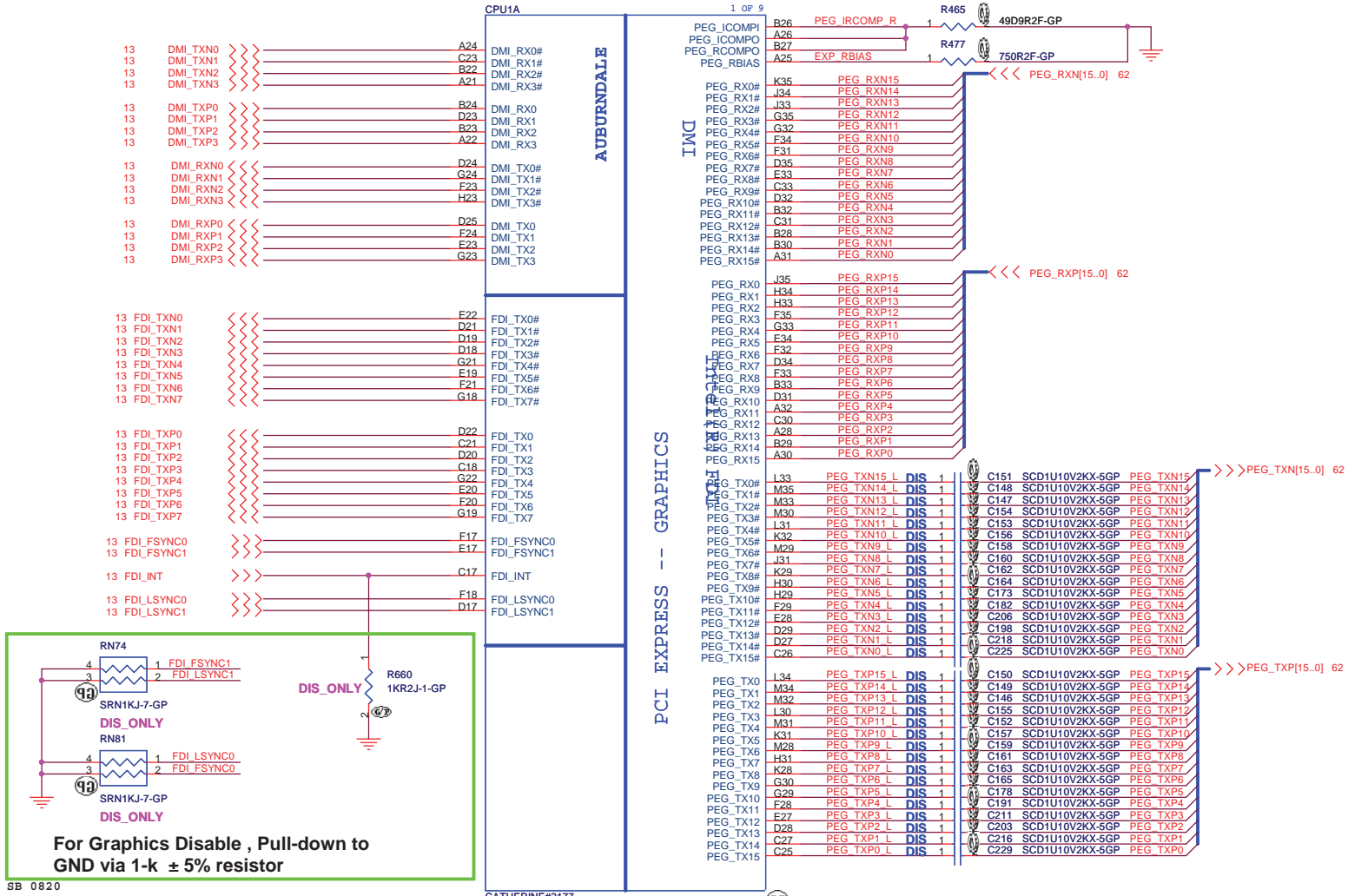
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

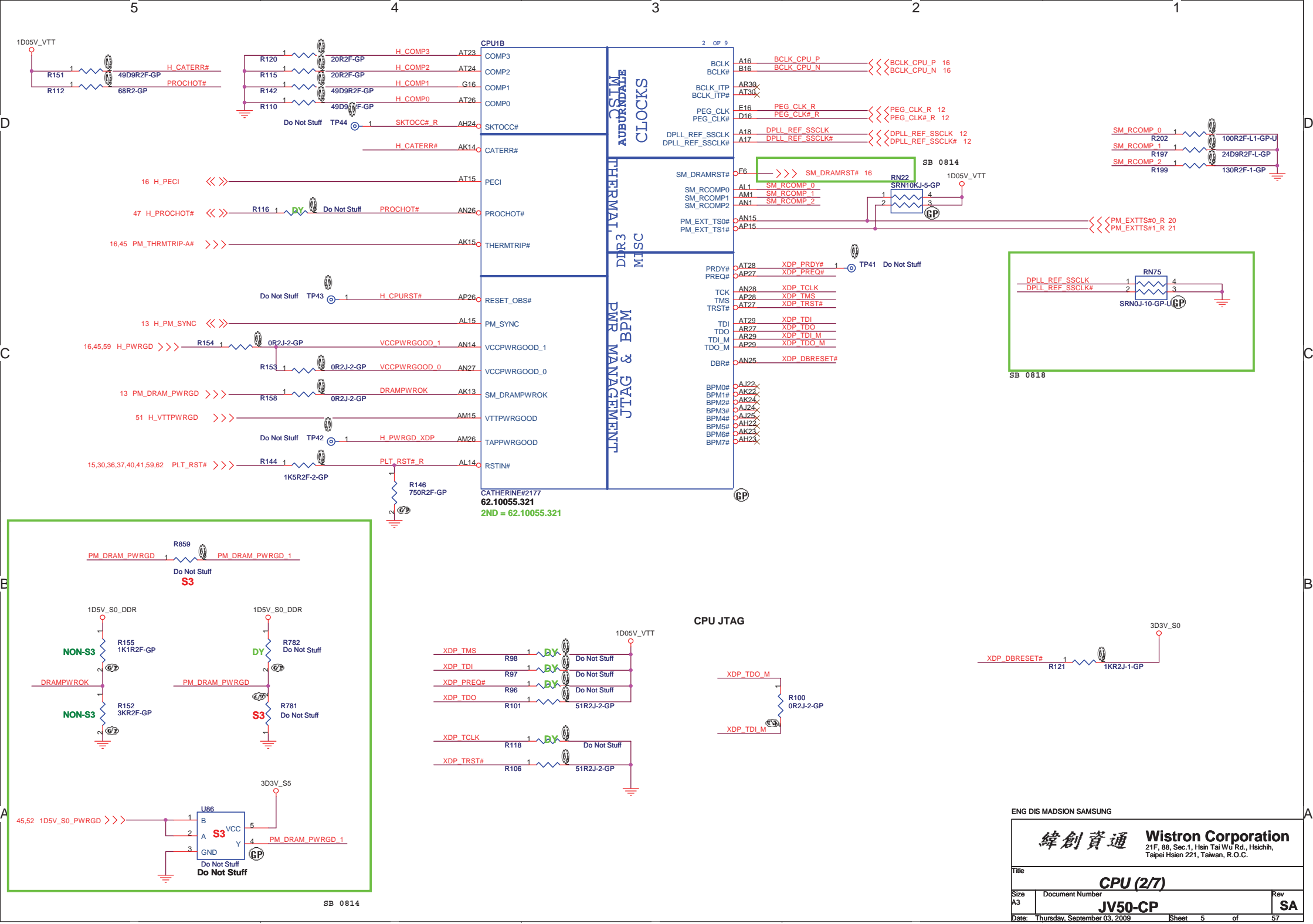
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

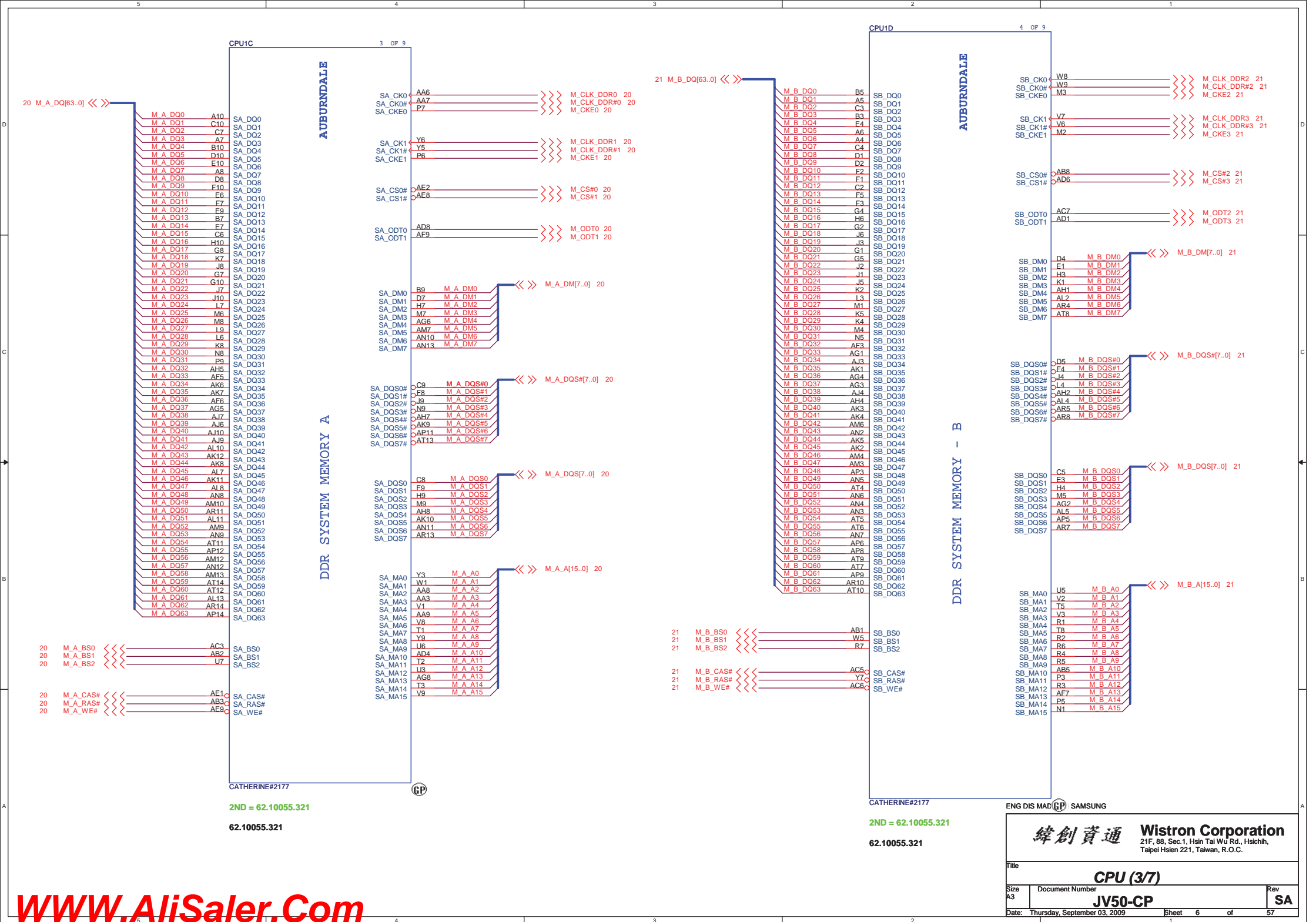
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Title			
Table of Content			
Size A3	Document Number JV50-CP	Rev	SA
Date	Tuesday, August 18, 2009	Sheet 2 of	57



62.10055.321
2ND = 62.10055.321

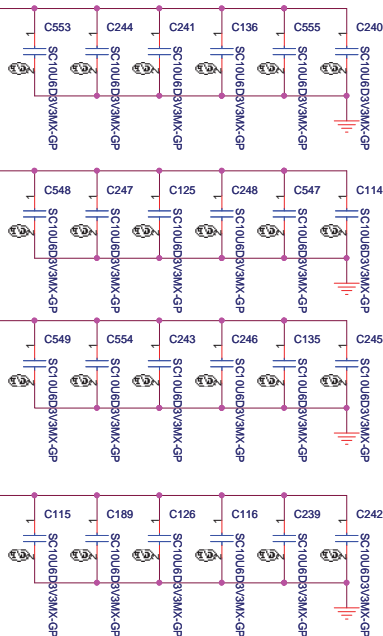




VCC_CORE

PROCESSOR CORE POWER

52A



VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

AUBURNDALE

1.1V RAIL

CPU CORE SUPPLY

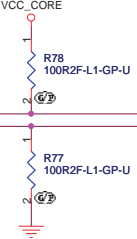
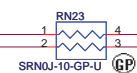
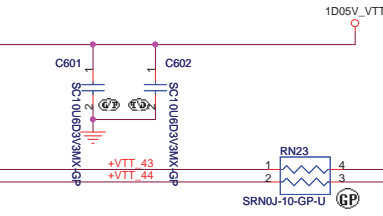
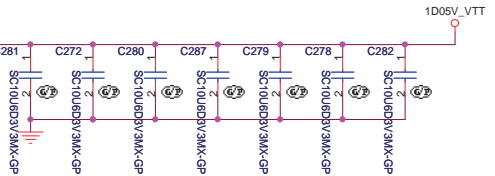
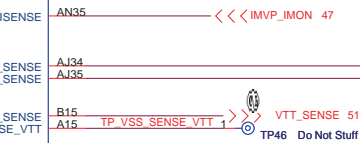
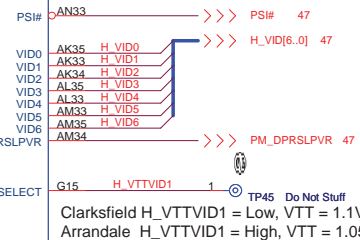
POWER

CPU VIDS

SENSE LINES

- VTT0 AH14
- VTT0 AH12
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 J13
- VTT0 H12
- VTT0 H11
- VTT0 G14
- VTT0 G13
- VTT0 G12
- VTT0 F14
- VTT0 F13
- VTT0 F12
- VTT0 E11
- VTT0 E12
- VTT0 D14
- VTT0 D13
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- VTT0 AF10
- VTT0 AE10
- VTT0 AC10
- VTT0 AB10
- VTT0 Y10
- VTT0 W10
- VTT0 U10
- VTT0 T10
- VTT0 J12
- VTT0 J11
- VTT0 J16
- VTT0 J15



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

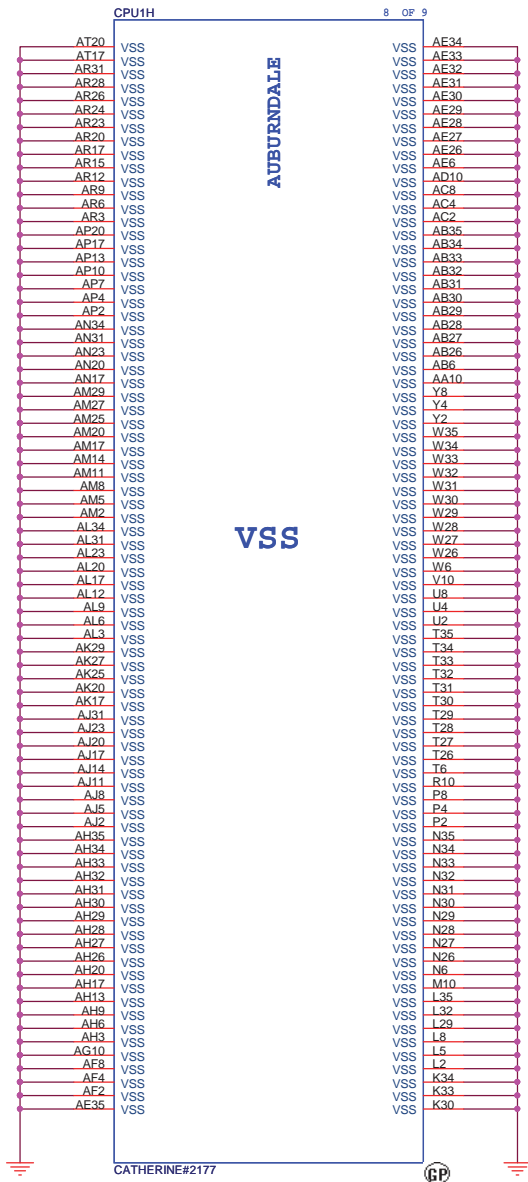
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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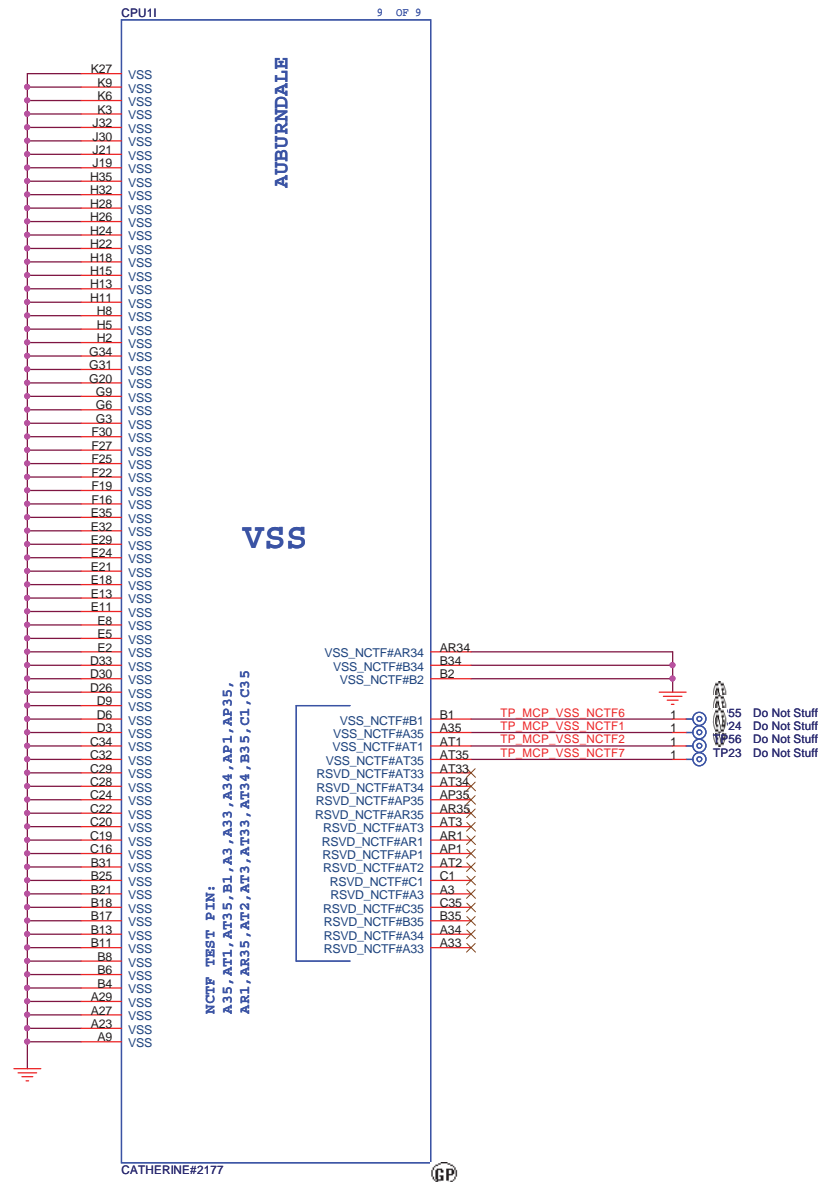
Title				
CPU (4/7)				
Size	Document Number			Rev
Custom	JV50-CP			SA
Date:	Thursday, September 03, 2009	Sheet	7	of 57

CATHERINE#2177
62.10055.321
2ND = 62.10055.321



2ND = 62.10055.321

62.10055.321



2ND = 62.10055.321

62.10055.321

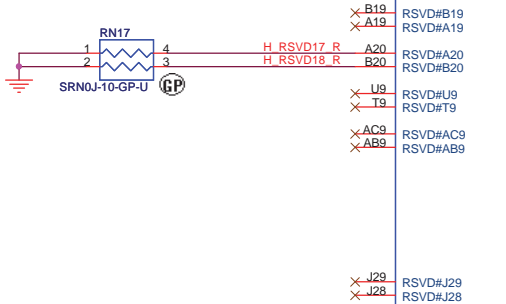
ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (6/7)		
Size A3	Document Number JV50-CP	Rev SA
Date: Wednesday, August 26, 2009	Sheet 9 of 57	

DY

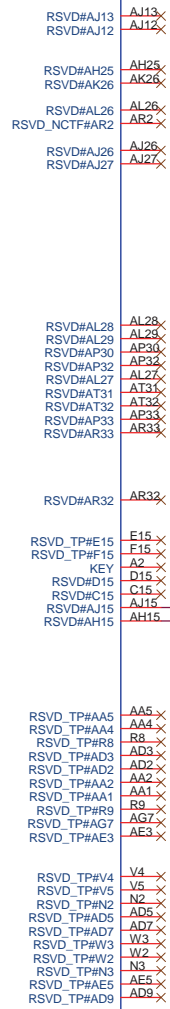
20 M_VREF_DQ_DIMM0 <<< 1 RN28 4 H RSDV9_R J17 RSVD#H28
21 M_VREF_DQ_DIMM1 <<< 2 3 H RSDV10_R H17 RSVD#H29
Do Not Stuff (CP) G17 RSVD#G25
G17 RSVD#G25
F31 RSVD#E31
F30 RSVD#E30

XG9 RSVD#AG9
M27 RSVD#M27
L28 RSVD#L28
SA_M_VREF# SA_M_VREF#
SB_DIMM_VREF# SB_DIMM_VREF#
XG25 RSVD#G25
G17 RSVD#G25
F31 RSVD#E31
F30 RSVD#E30

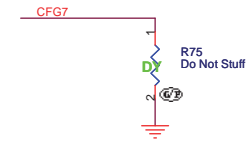
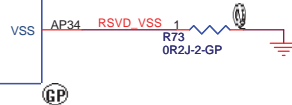


5 OF 9

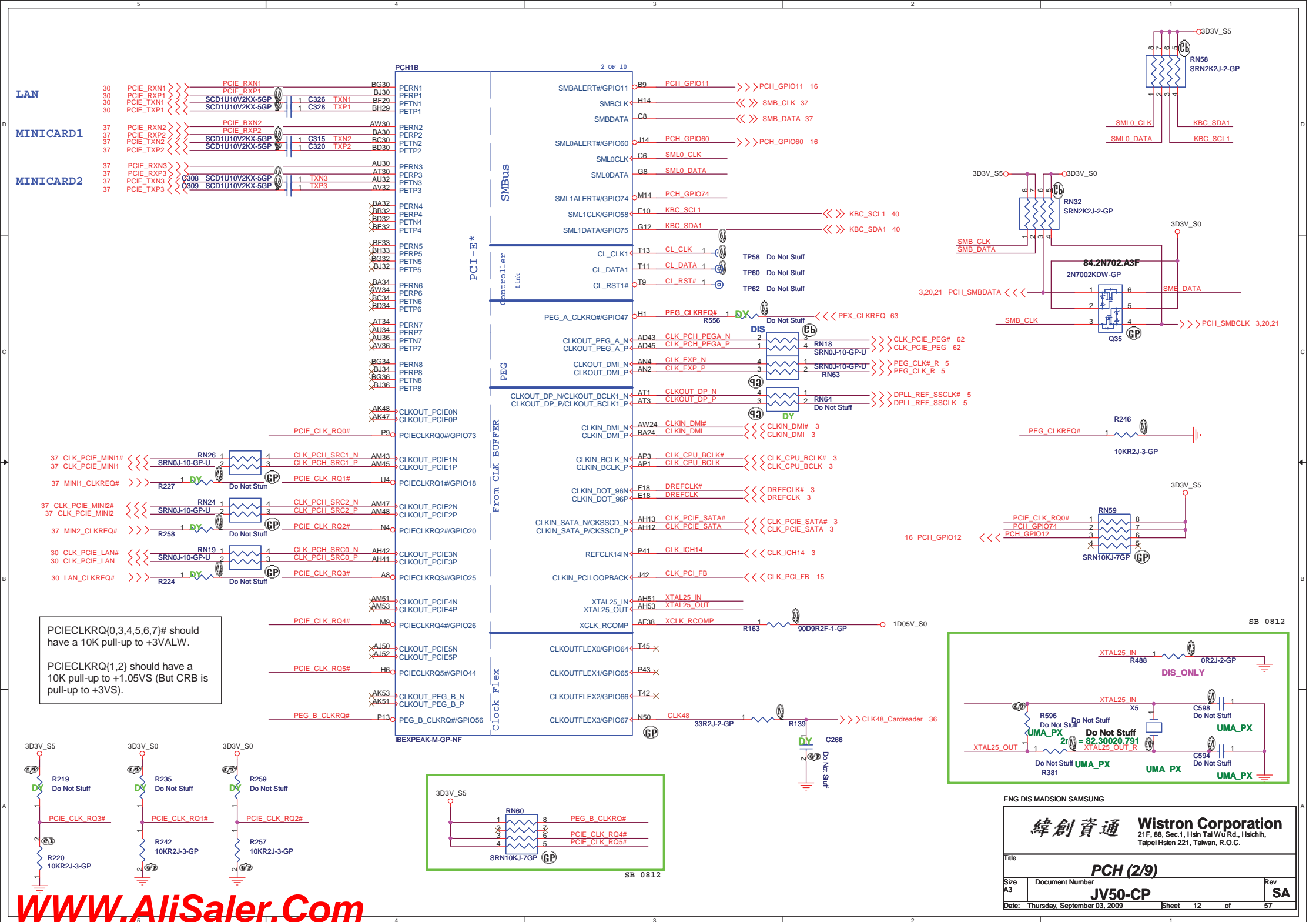
RESERVED

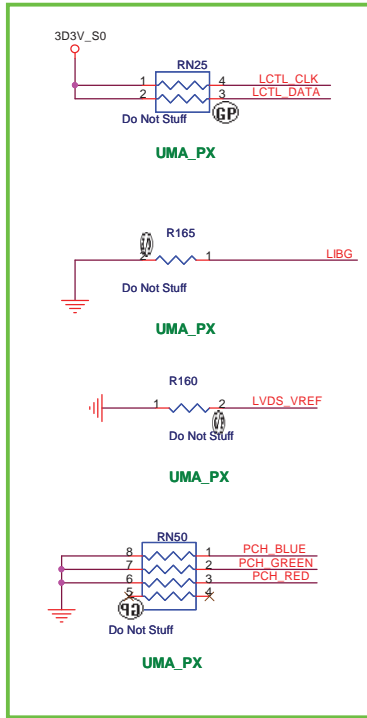


VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

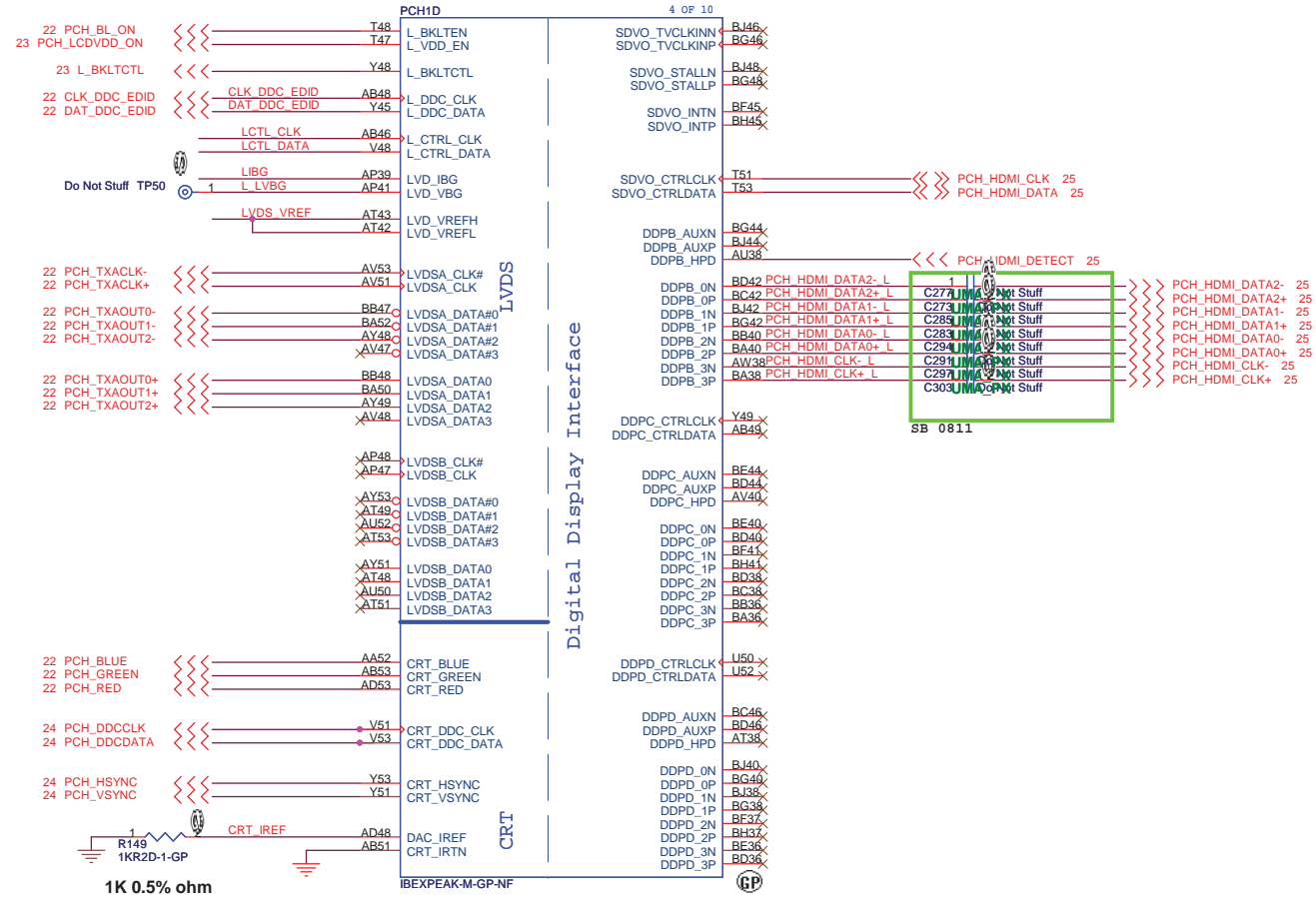


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report].</p> <p>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>





SB 0811

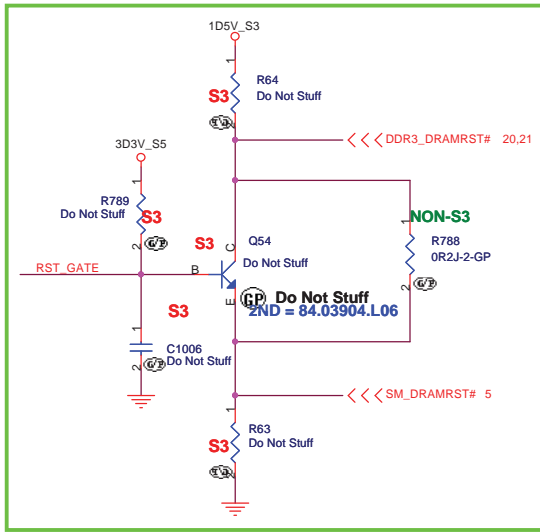
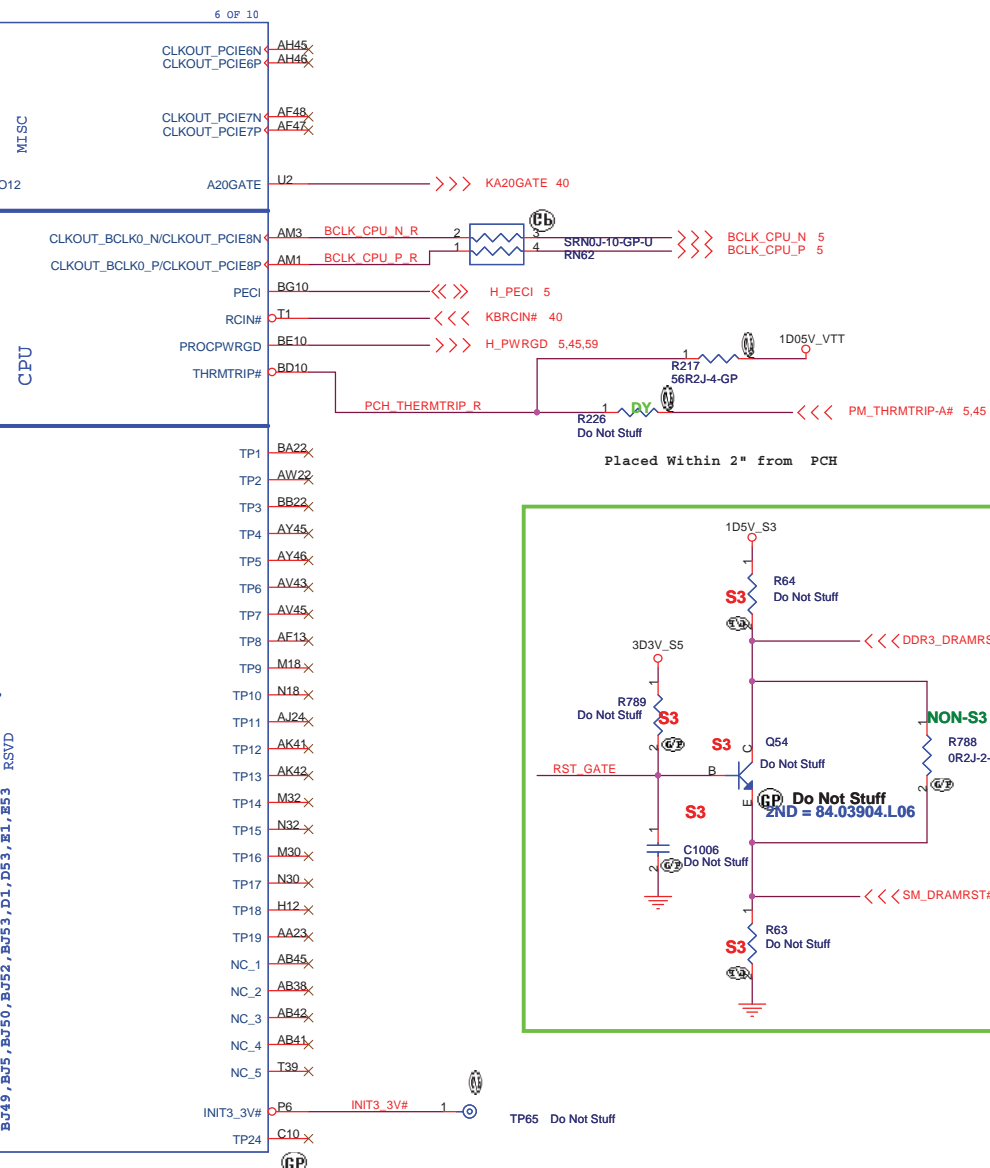
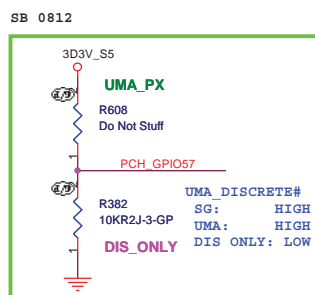
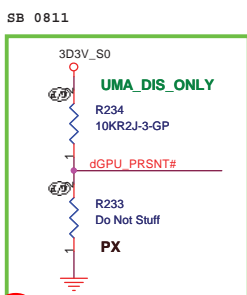
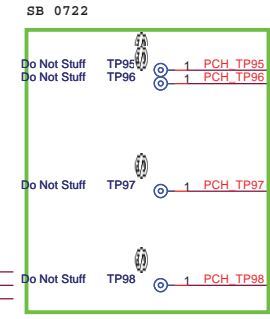
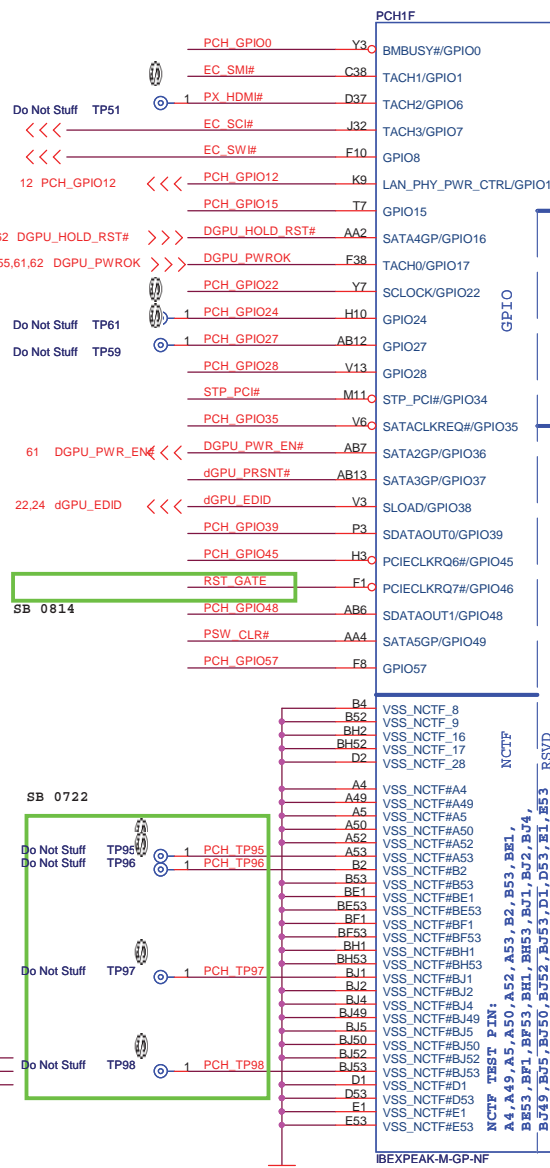
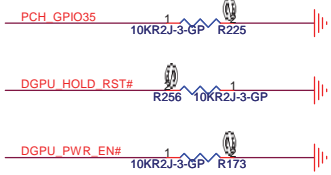
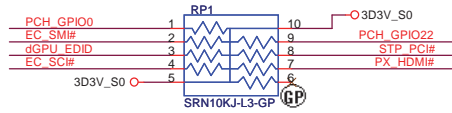
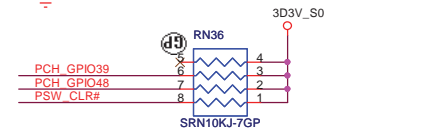
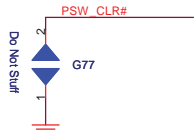


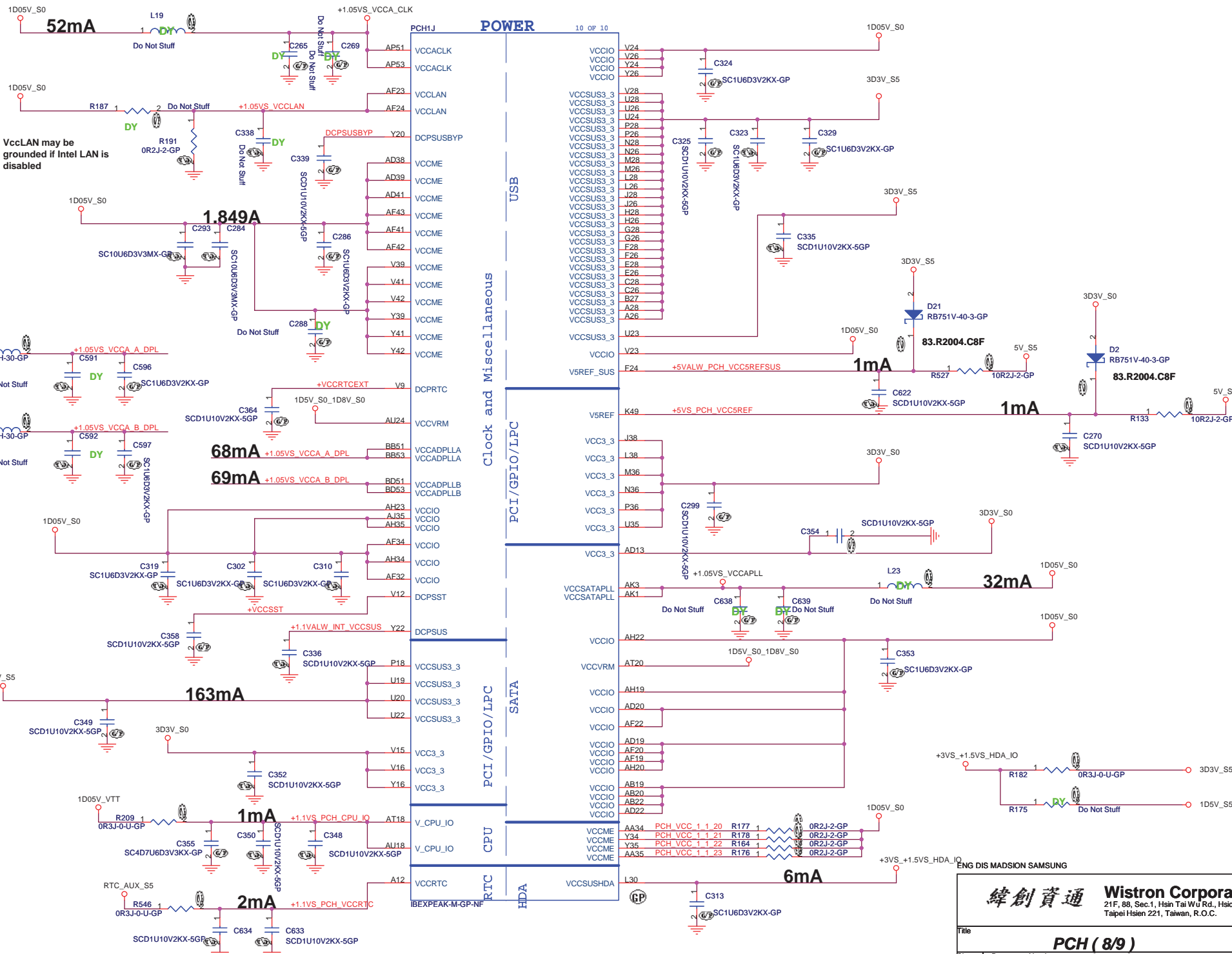
ENG DIS MADSION SAMSUNG

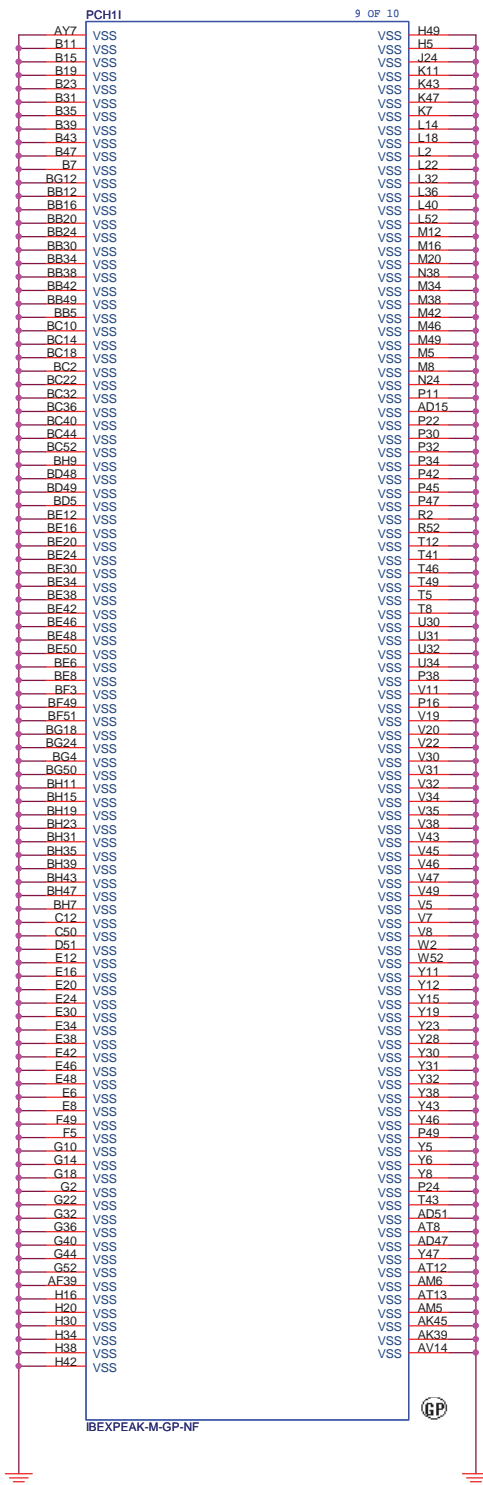
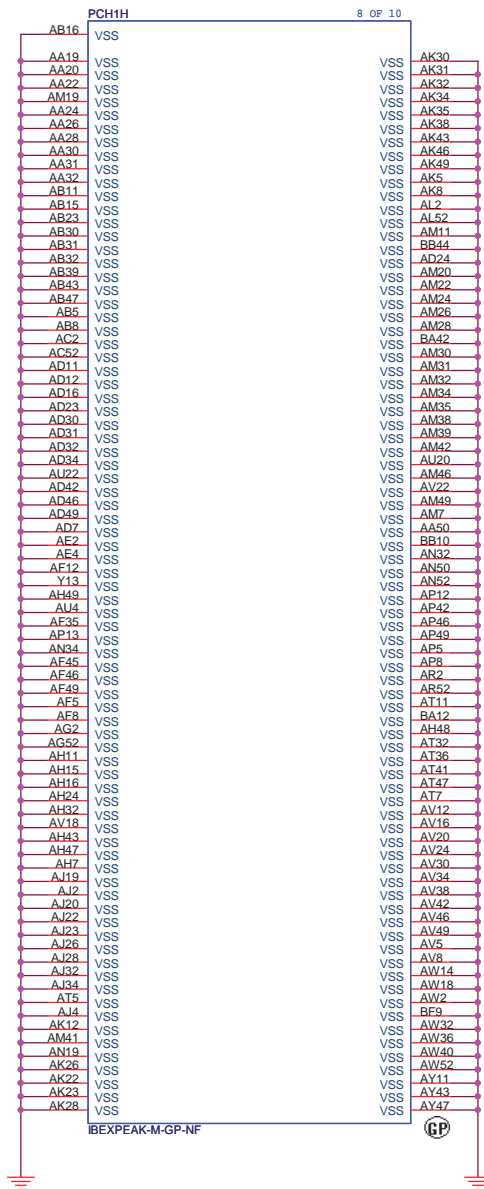
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Title	PCH (4/9)		
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GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.







SB 0818

SB 0817

SB 0817

SB 0817

**Place these caps
close to VTT1 and
VTT2.**

10 M_VREF_DQ_DIMM0
16,21 DDR3_DRAMRST#

REVERSE TYPE

Layout Note:
Place these Caps near
SQ-DIMMA

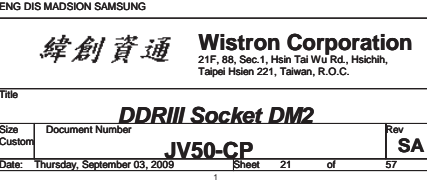
Note:
 If SA0_DIM0 = 0, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA0
 SO-DIMMA TS Address is 0x30

 If SA0_DIM0 = 1, SA1_DIM0 = 0
 SO-DIMMA SPD Address is 0xA2
 SO-DIMMA TS Address is 0x32

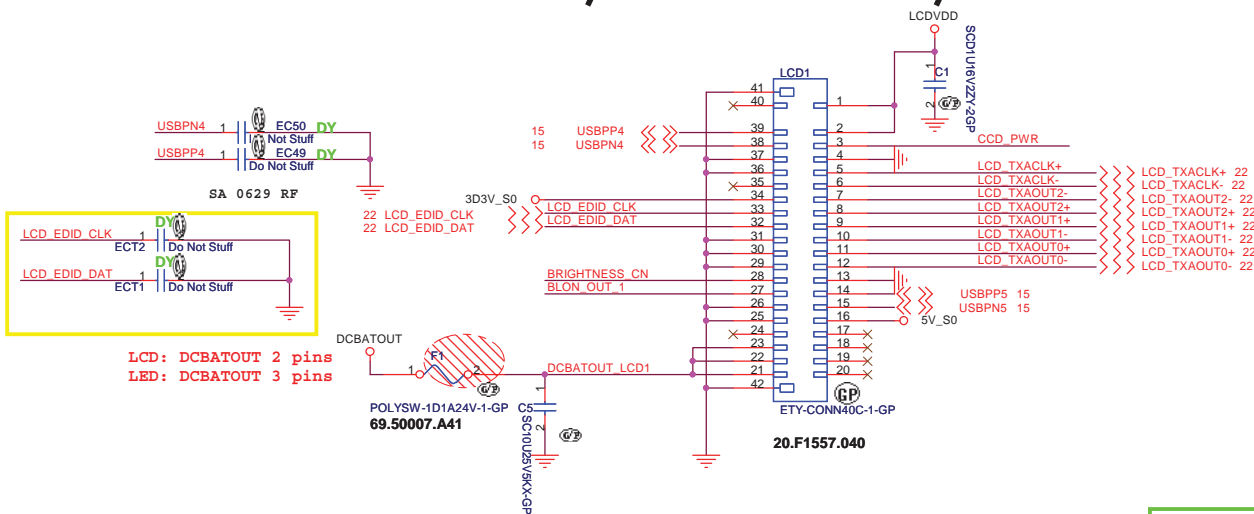
SODIMM A DECOUPLING

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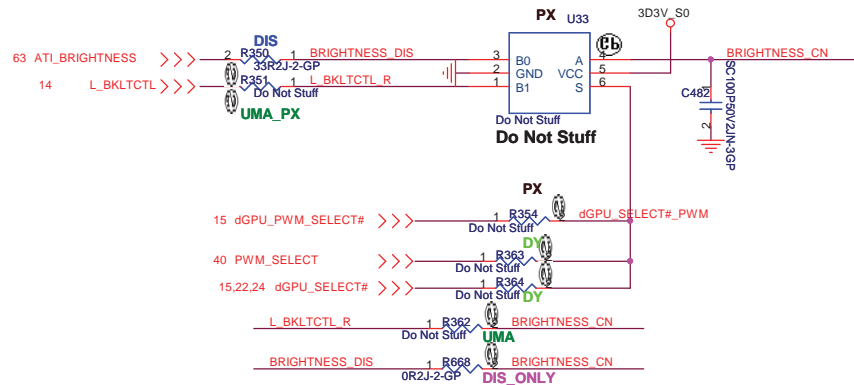
LCD/INVERTER/CCD CONN



SA 0702 EMI

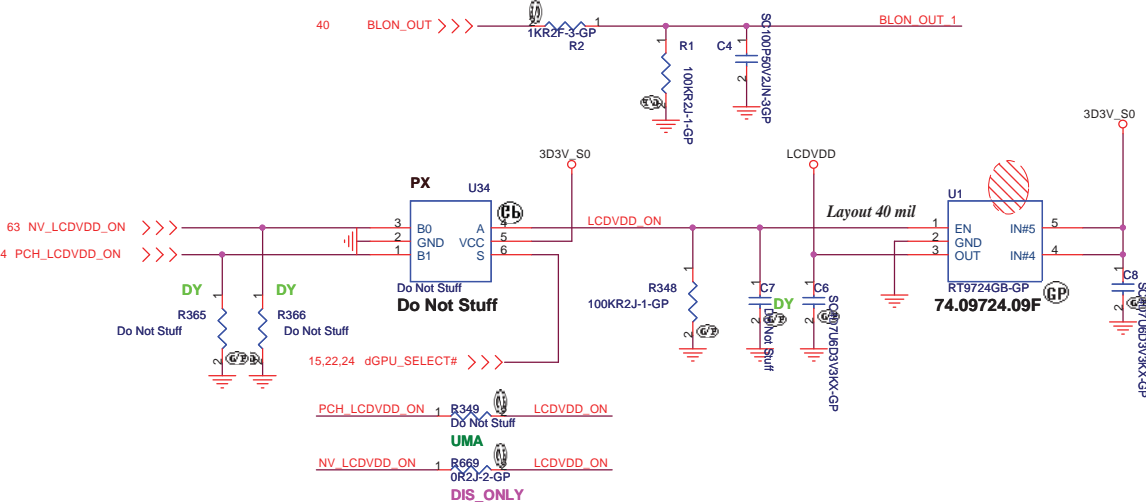
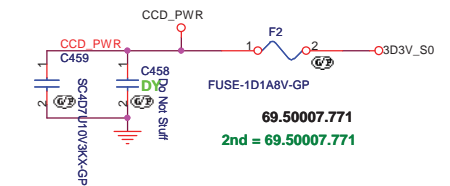
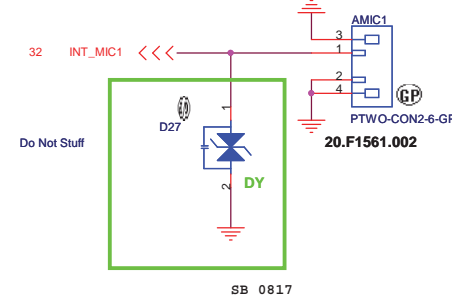


modify by RF



SB 0812

Internal Mic

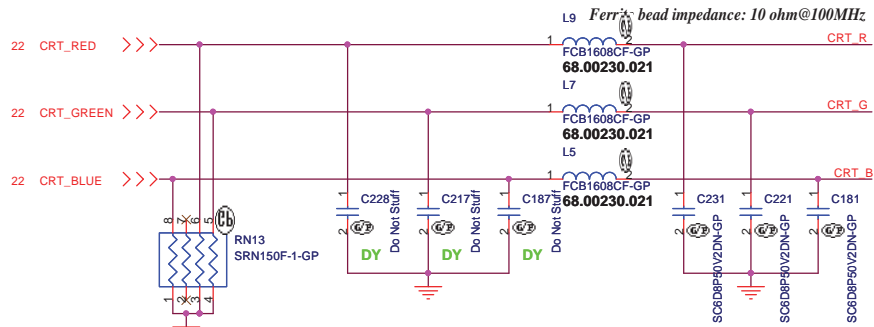


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LCD CONN			
Size	Document Number	JV50-CP	
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Layout Note:
Place these resistors
close to the CRT-out
connector

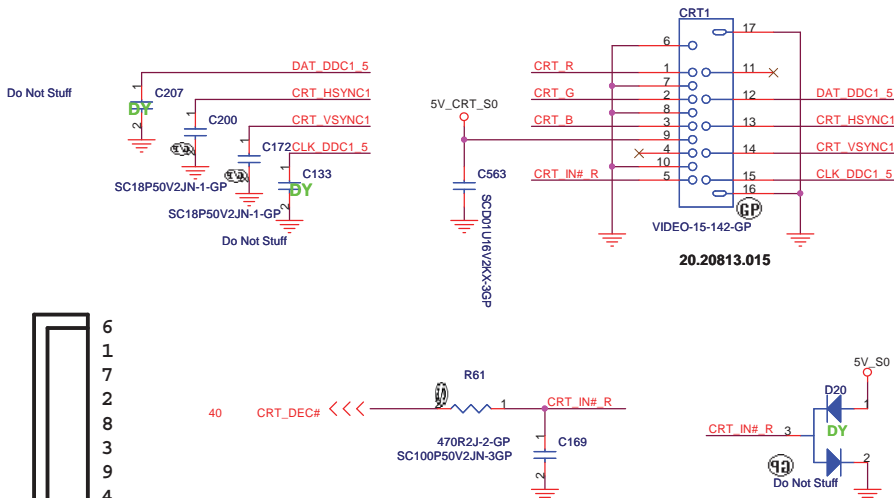


Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#

For DIS CRT

63,66 NV_CRT_HSYNC

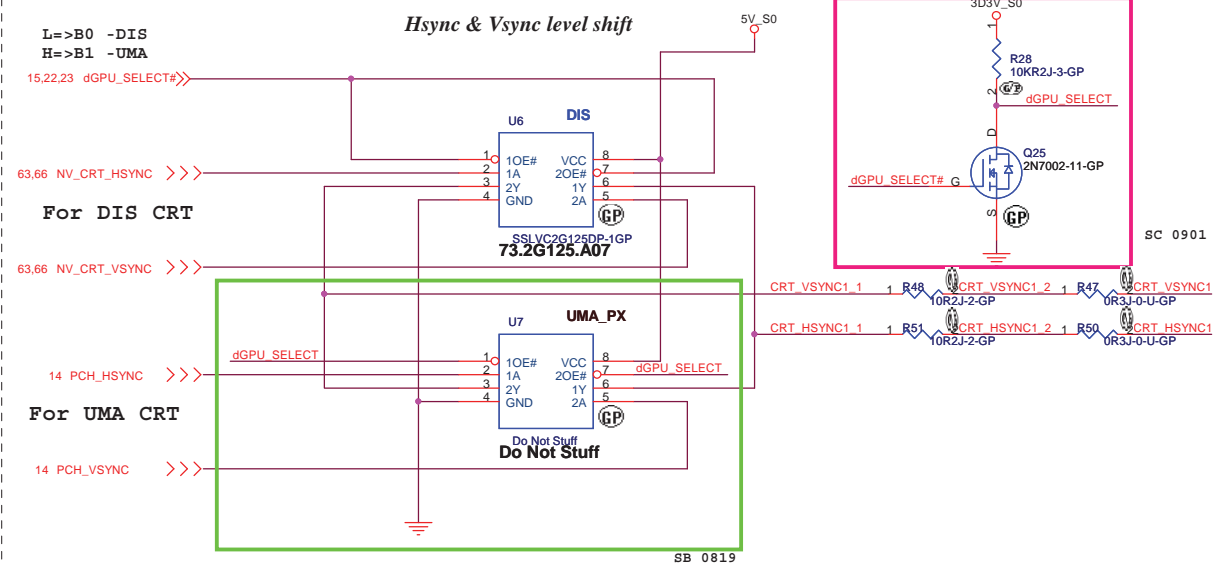
63,66 NV_CRT_VSYNC

For UMA CRT

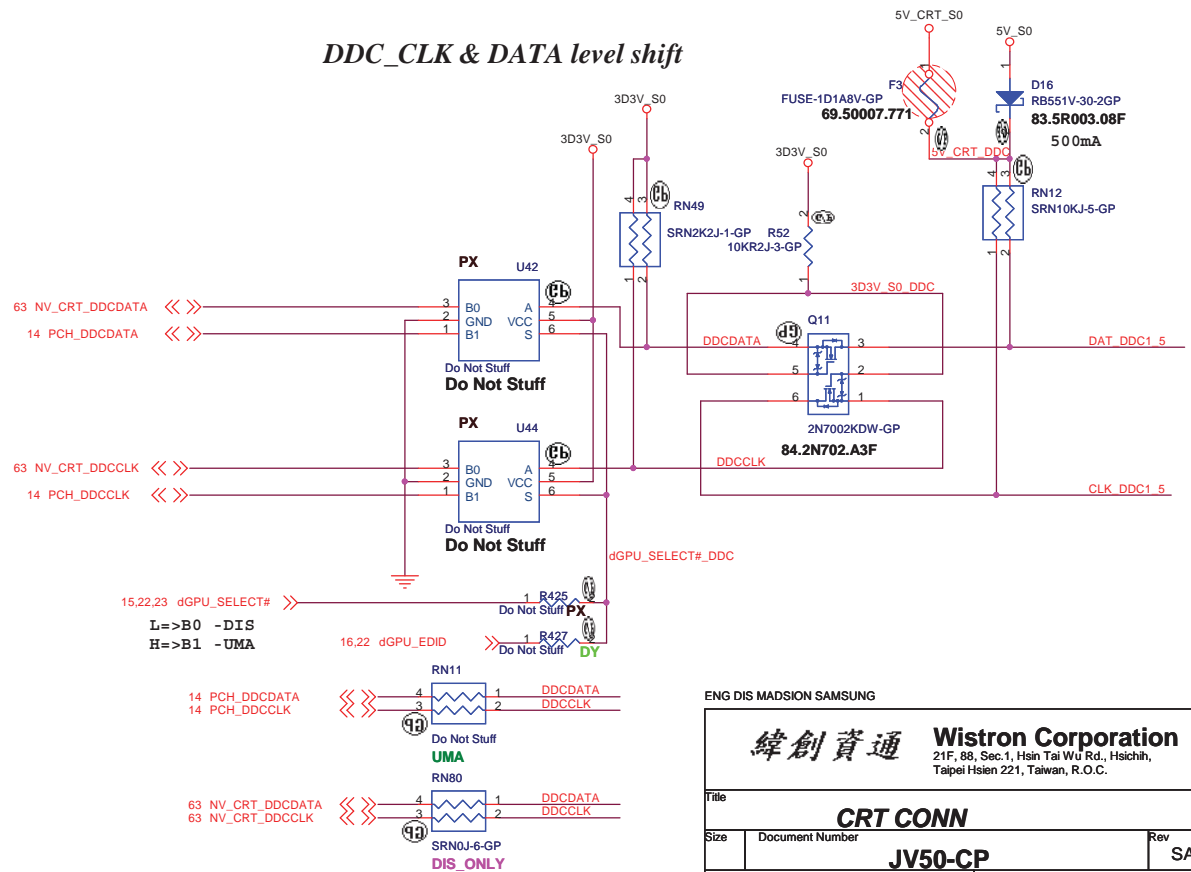
14 PCH_HSYNC

14 PCH_VSYNC

Hsync & Vsync level shift



DDC_CLK & DATA level shift



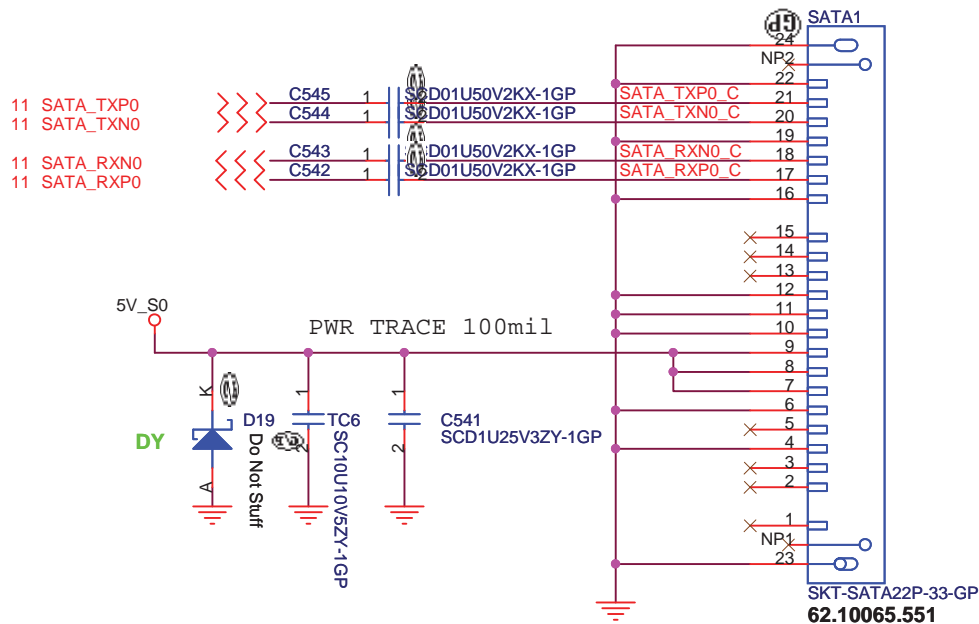
ENG DIS MADSION SAMSUNG

緯創資通

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Title			CRT CONN	
Size	Document Number	JV50-CP		Rev
Date: Thursday, September 03, 2009		Sheet	24	of 61

SATA Connector



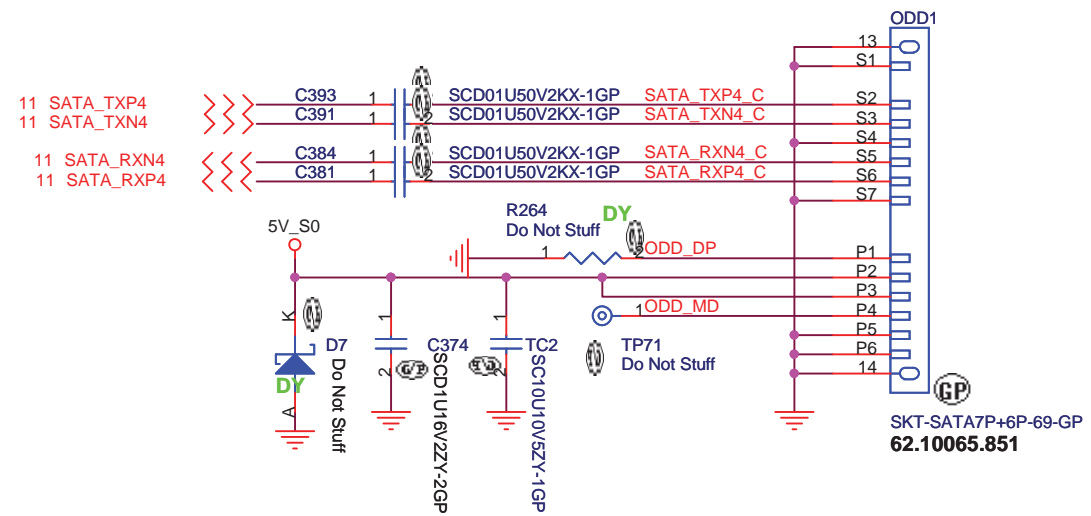
ENG DIS MADSION SAMSUNG

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Title			HDD CONN	
Size	Document Number		JV50-CP	
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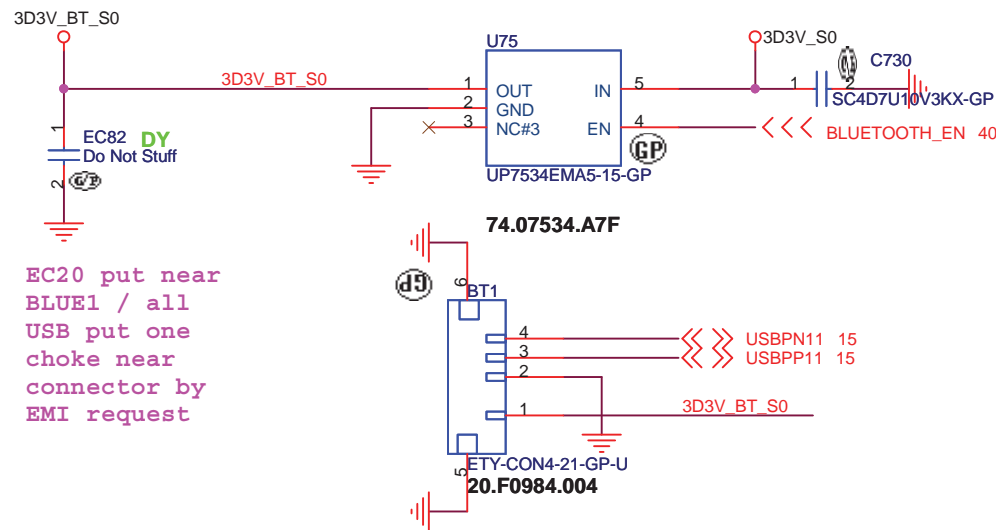
ODD Connector



ENG DIS MADSION SAMSUNG

緯創資通		Wistron Corporation	
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Title			
ODD			
Size	Document Number		Rev
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BLUETOOTH MODULE



ENG DIS MADSION SAMSUNG

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLUETOOTH

Size

Document Number

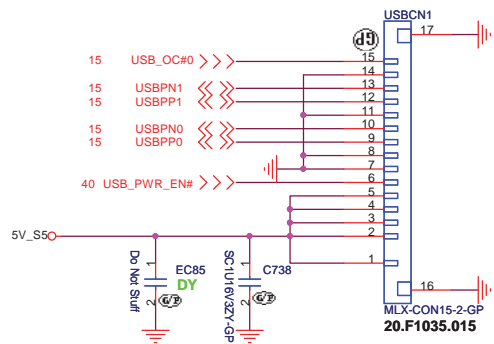
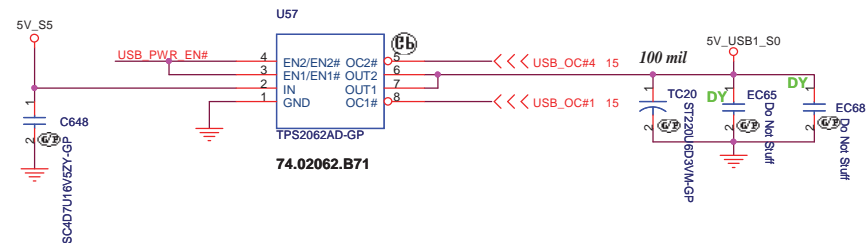
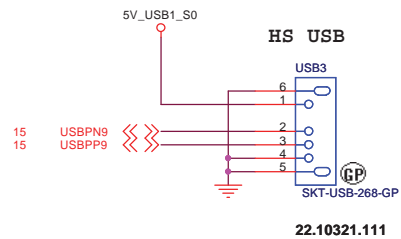
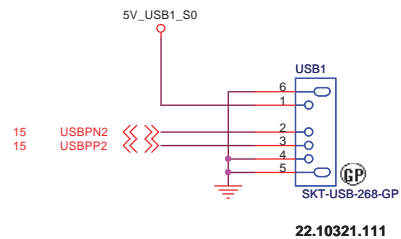
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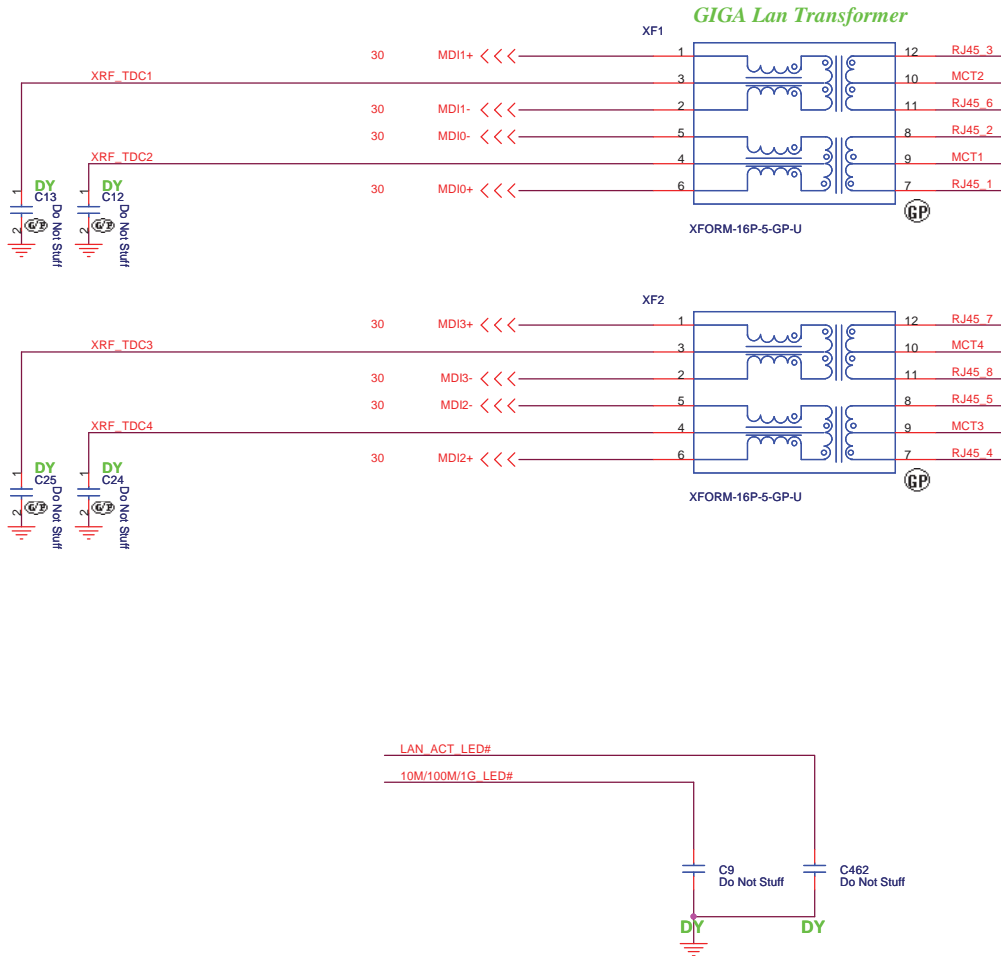


ENG DIS MADSION SAMSUNG

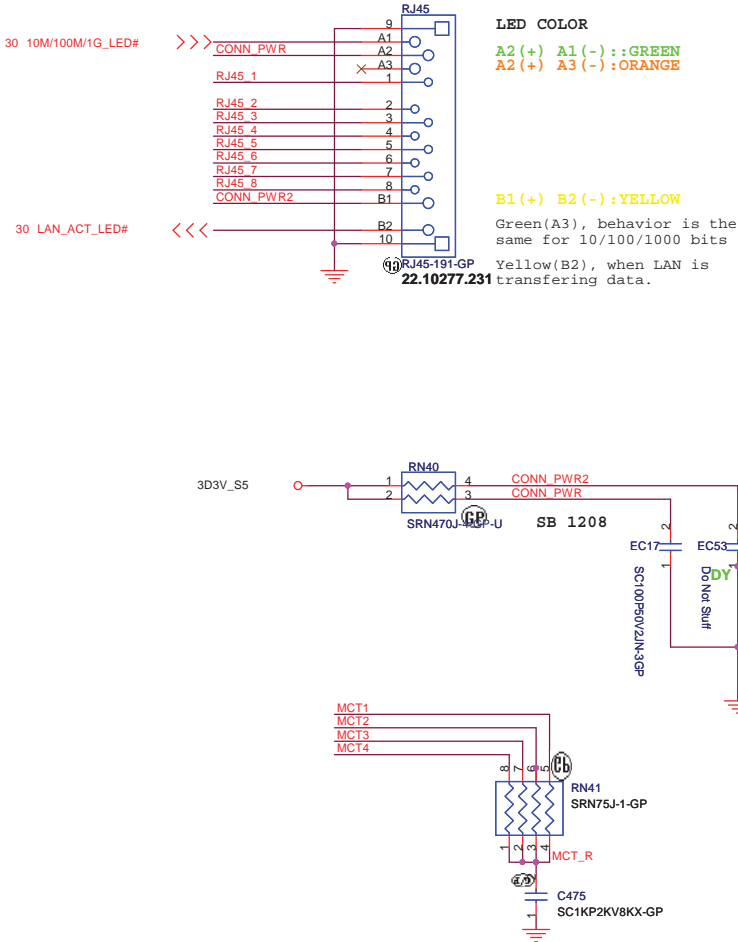
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
USB CONN			
Size	Document Number	Rev	SA
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

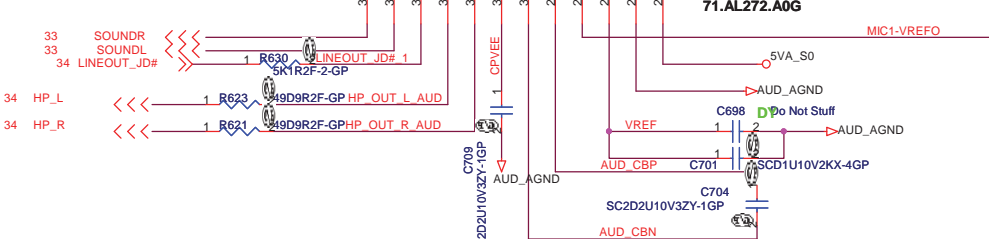
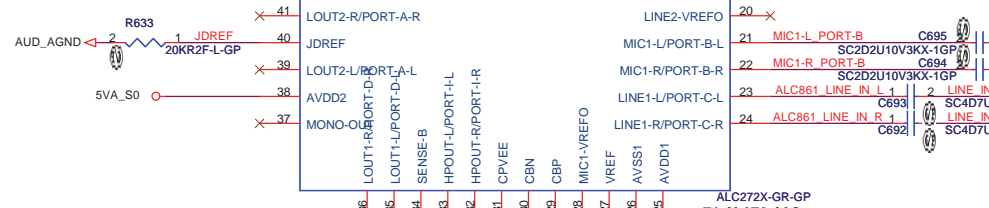
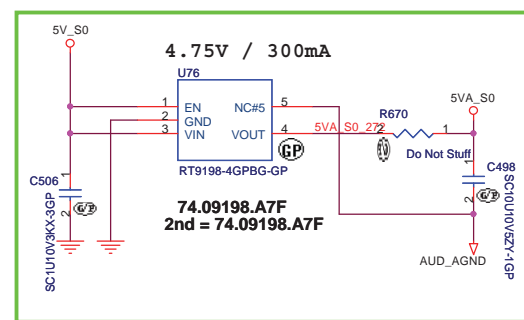
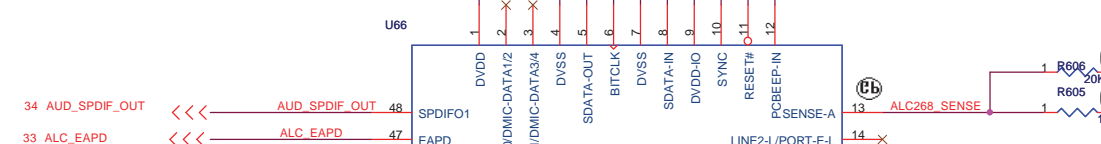
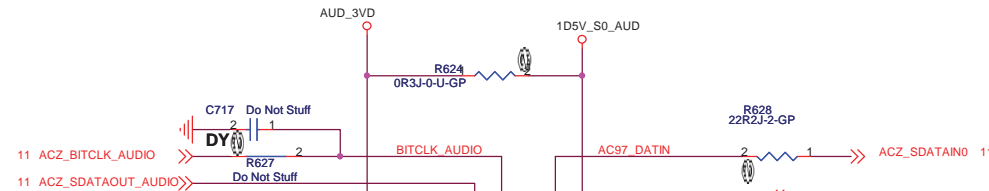
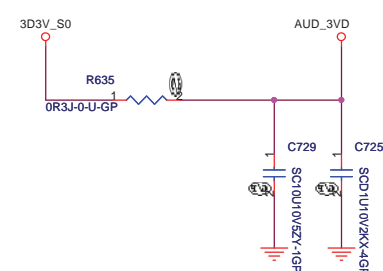
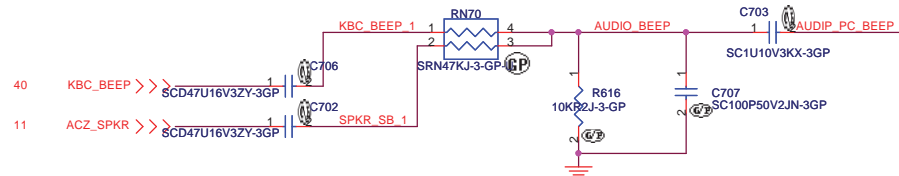


LAN Connector



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title LAN CONN		
Size A3	Document Number JV50-CP	Rev SA
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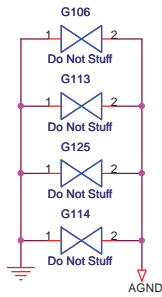
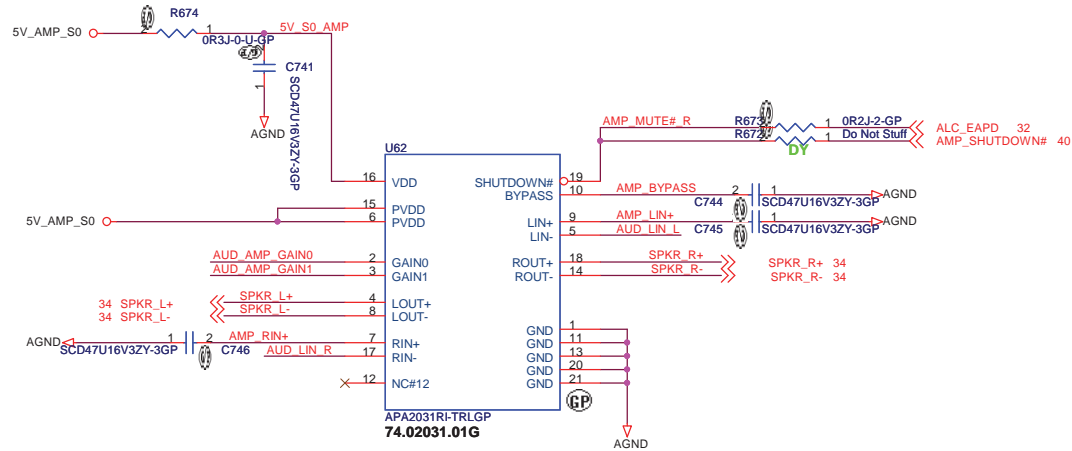
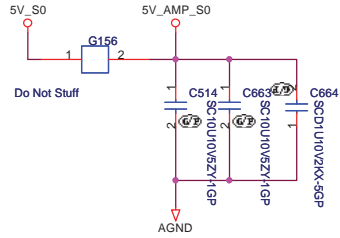
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

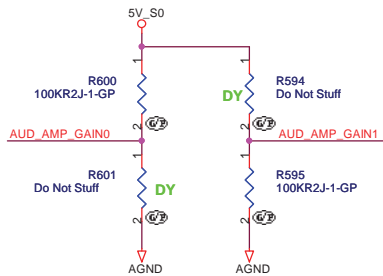
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Size A3 Document Number **JV50-CP** Rev **SA**

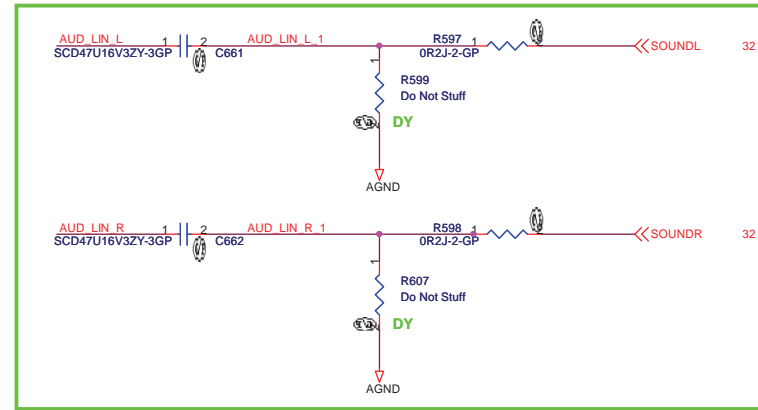
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GAIN SETTING



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

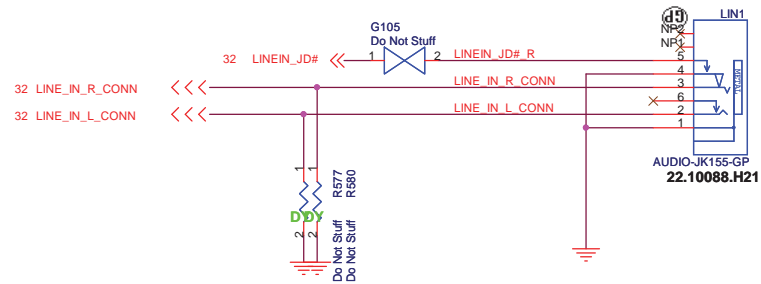


SB 0814

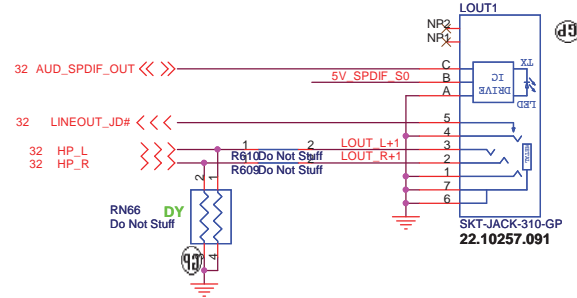
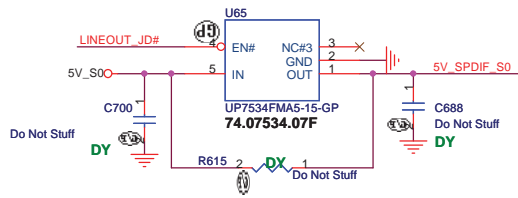
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
AUDIO AMP		
Size	Document Number	Rev
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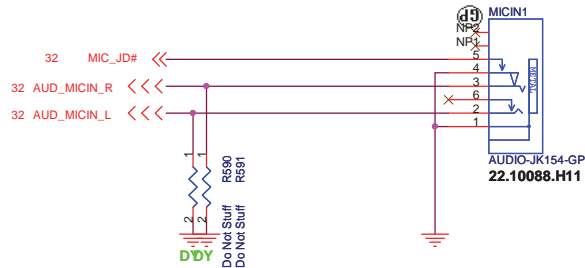
LINE IN



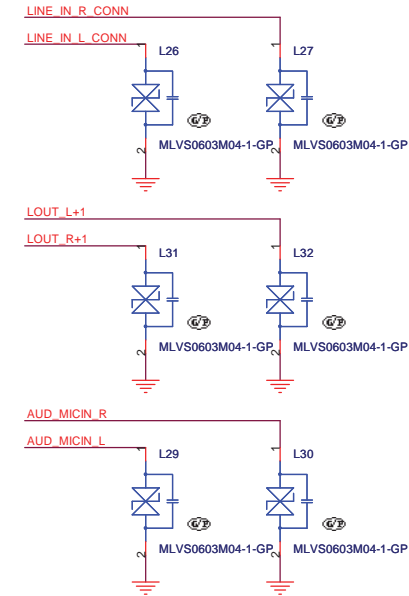
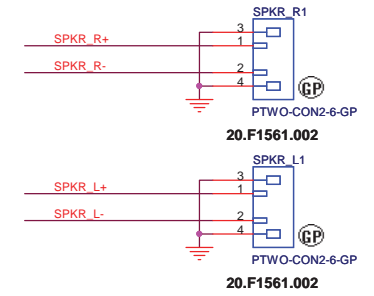
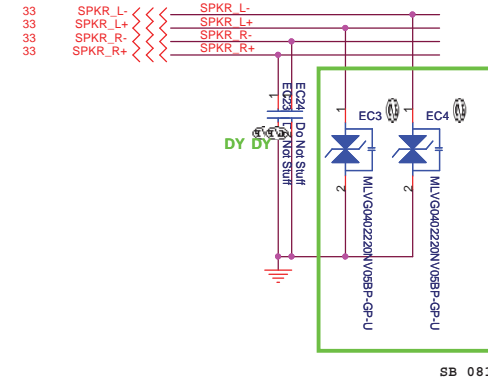
LINE OUT



MIC IN



Internal Speaker

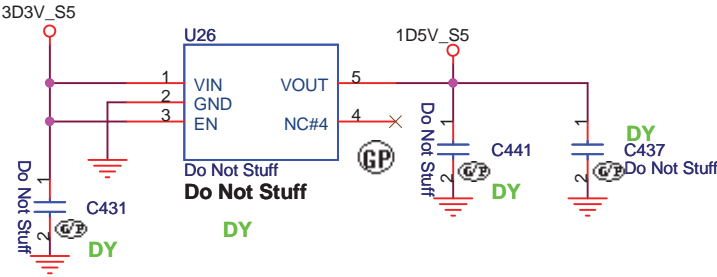
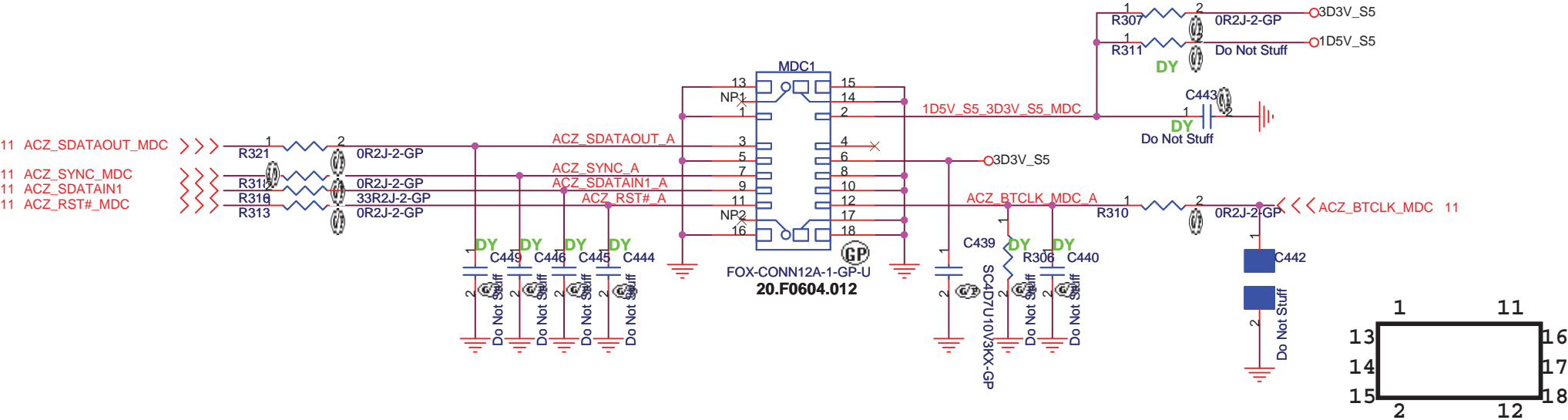


ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

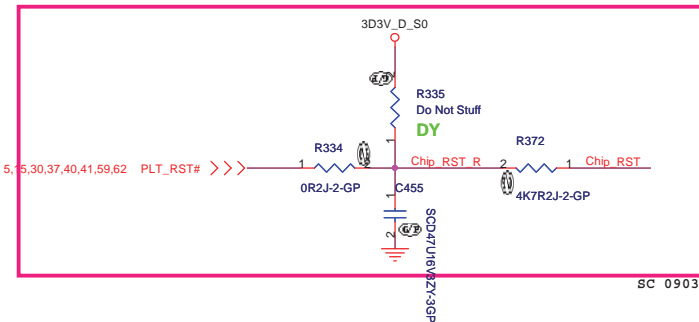
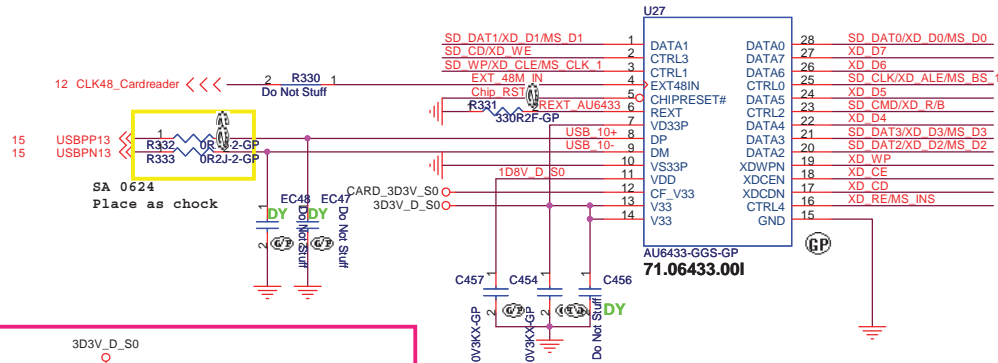
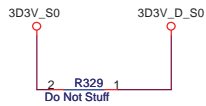
Title			AUDIO jack
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MDC 1.5 CONN

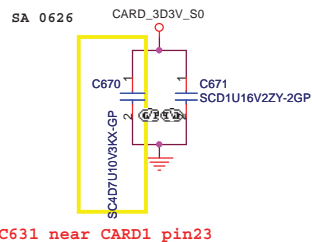


ENG DIS MADSION SAMSUNG

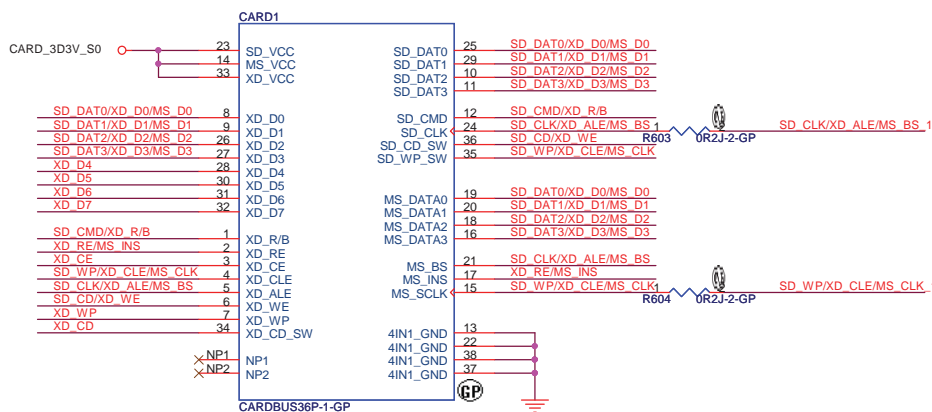
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



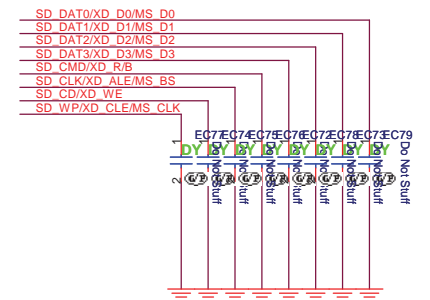
C631 near CARD1 pin23



2nd = 20.10079.011

20.10109.001

EMI capacitor

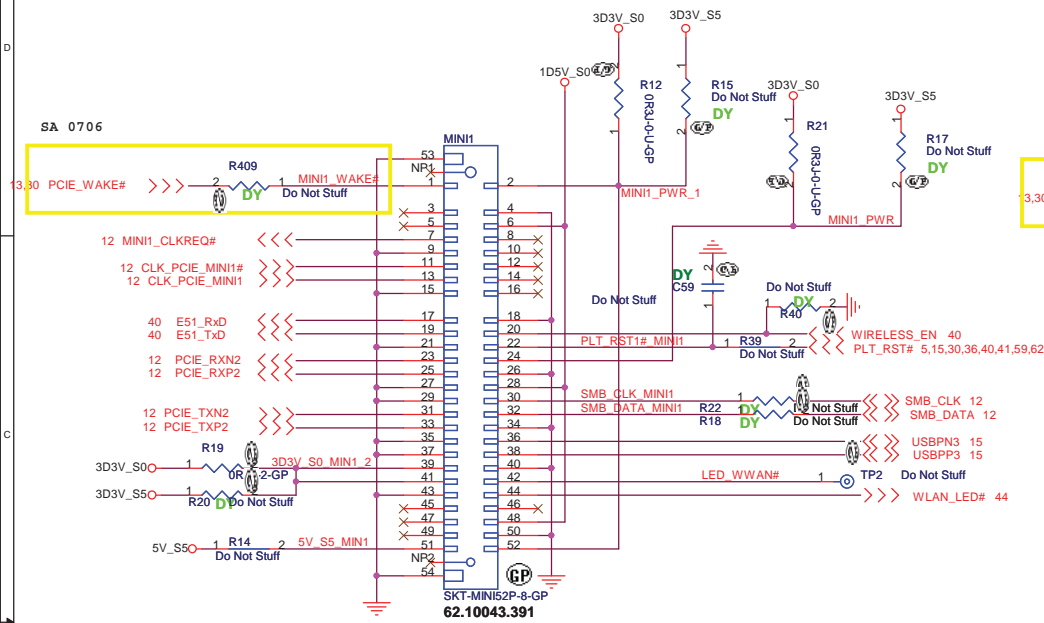


ENG DIS MADISON SAMSUNG

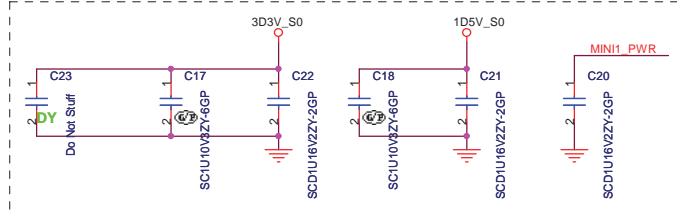
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			Cardreader
Size	Document Number	Rev	SA
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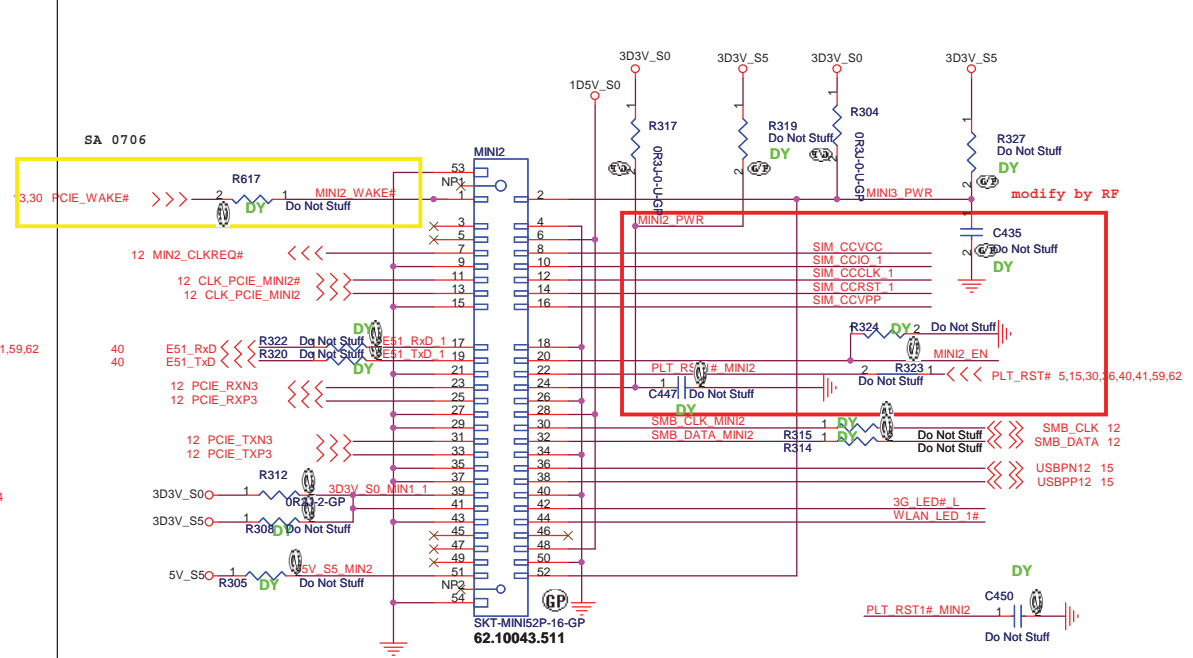
Mini Card Connector(WLAN)



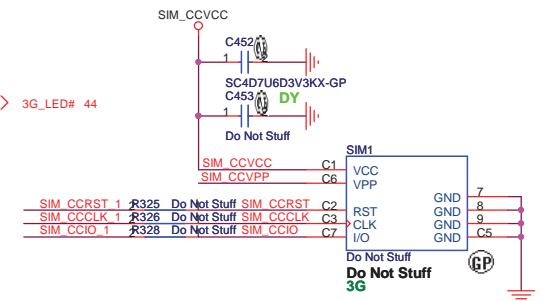
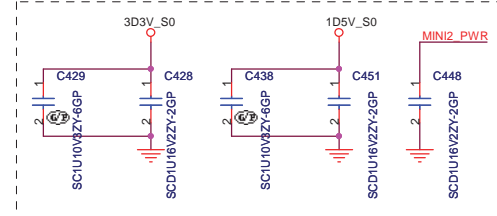
Place near MINI1



Mini Card Connector(Robson2 and 3G)



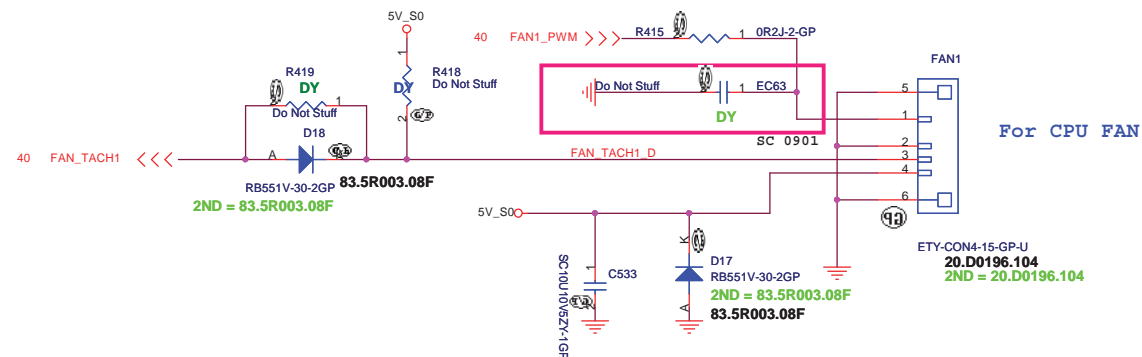
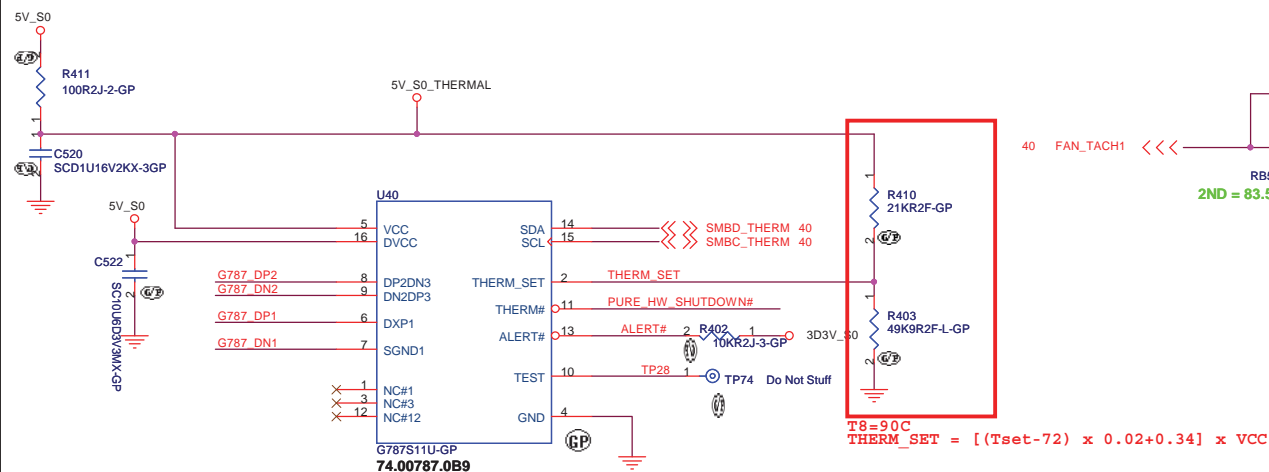
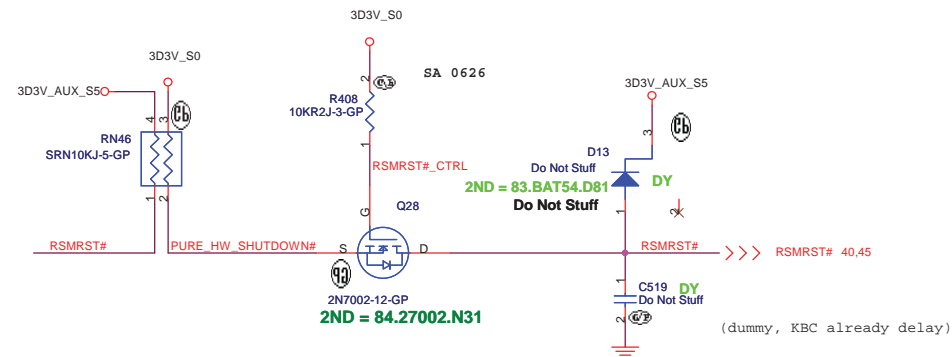
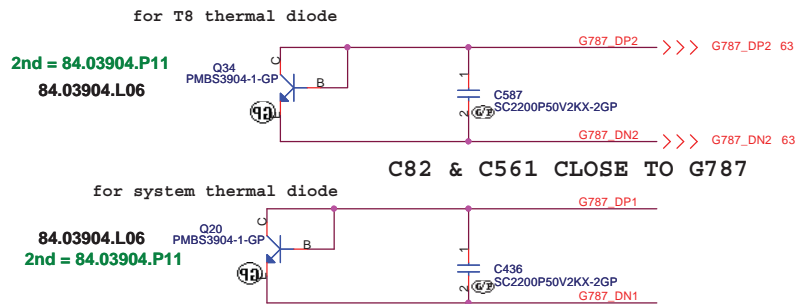
Place near MINIC2



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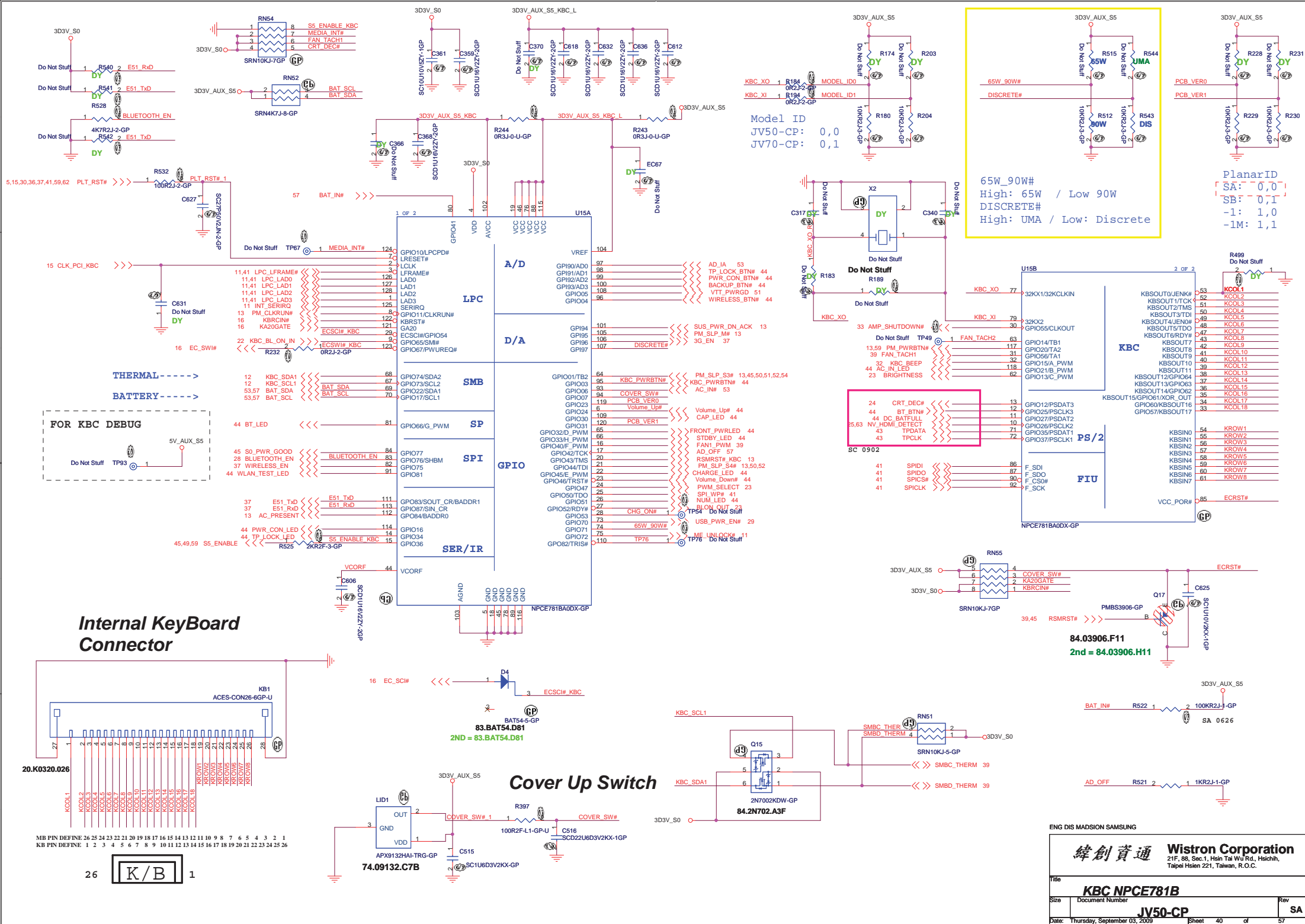
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MINI CARD			
Size A3	Document Number	Rev	
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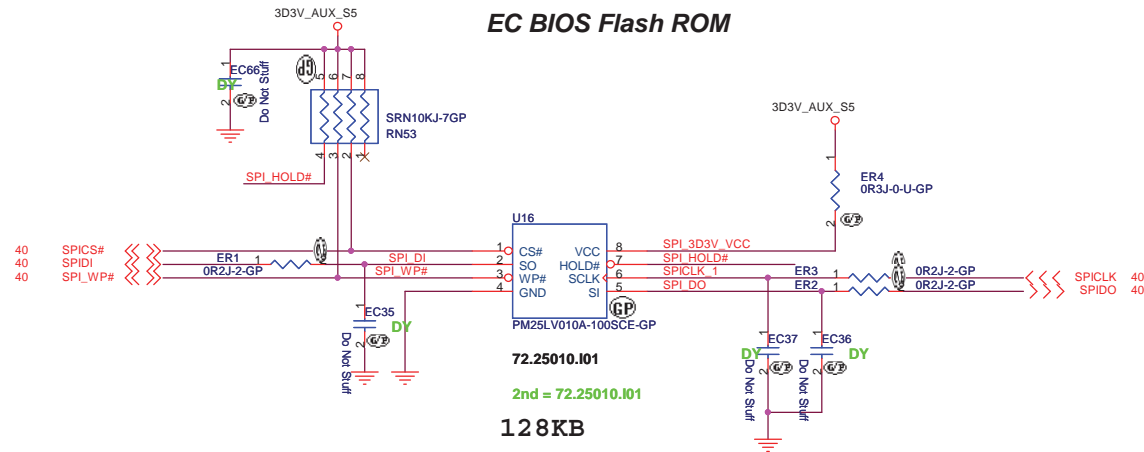
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

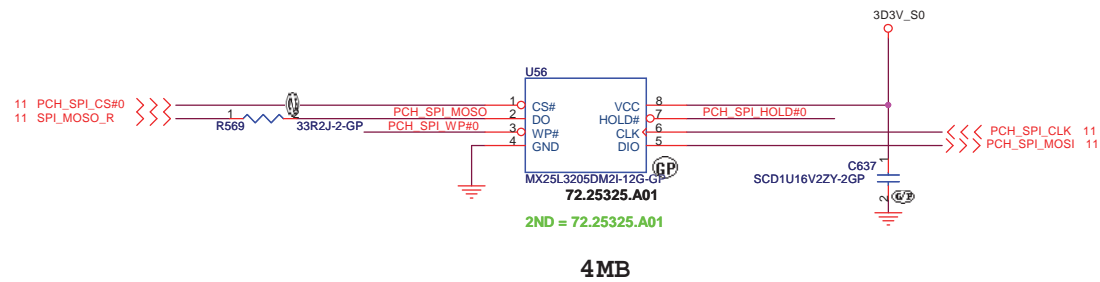
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Thermal/Fan Connector			
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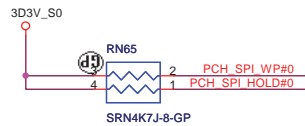
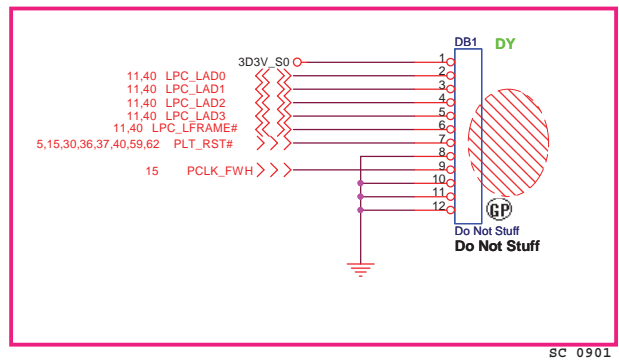
EC BIOS Flash ROM



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD

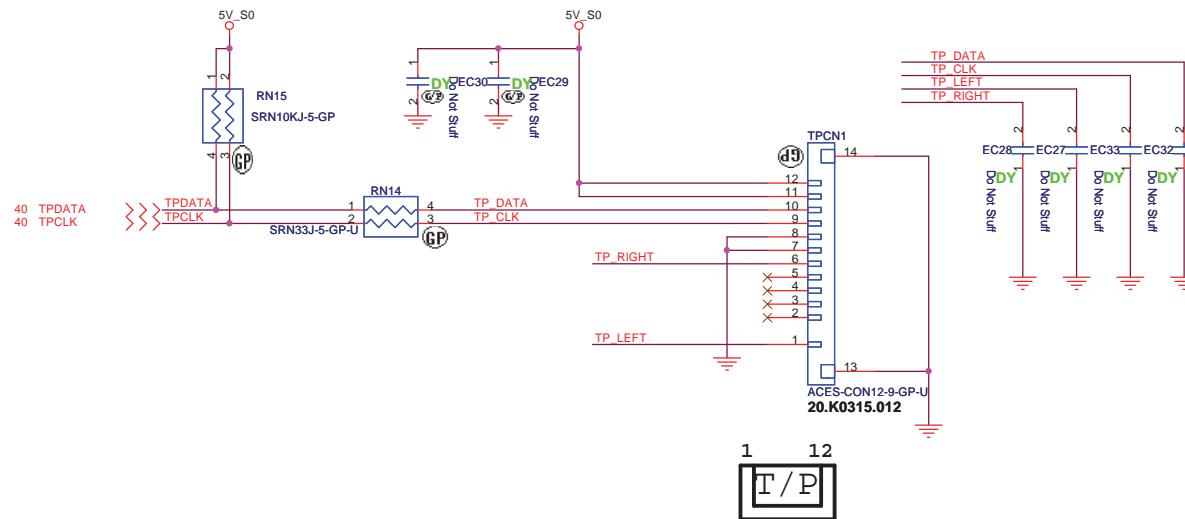


ENG DIS MADSION SAMSUNG

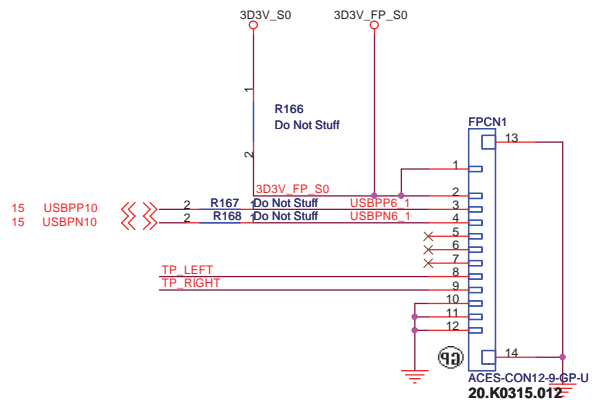
緯創資通 Wistron Corporation
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TOUCH PAD



Finger printer



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緯創資通

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Title

Touch PAD and FP

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FRONT_PWRLED#_Q 4
STDBY_LED#_Q 3
DC_BATFULL#_Q 2
CHARGE_LED#_Q 1

LED-BY-GP
83.00195.J70

CHARGER_LED1

DC_BATFULL#_R

5V_AUX



ENG DIS MADSION SAMSUNG

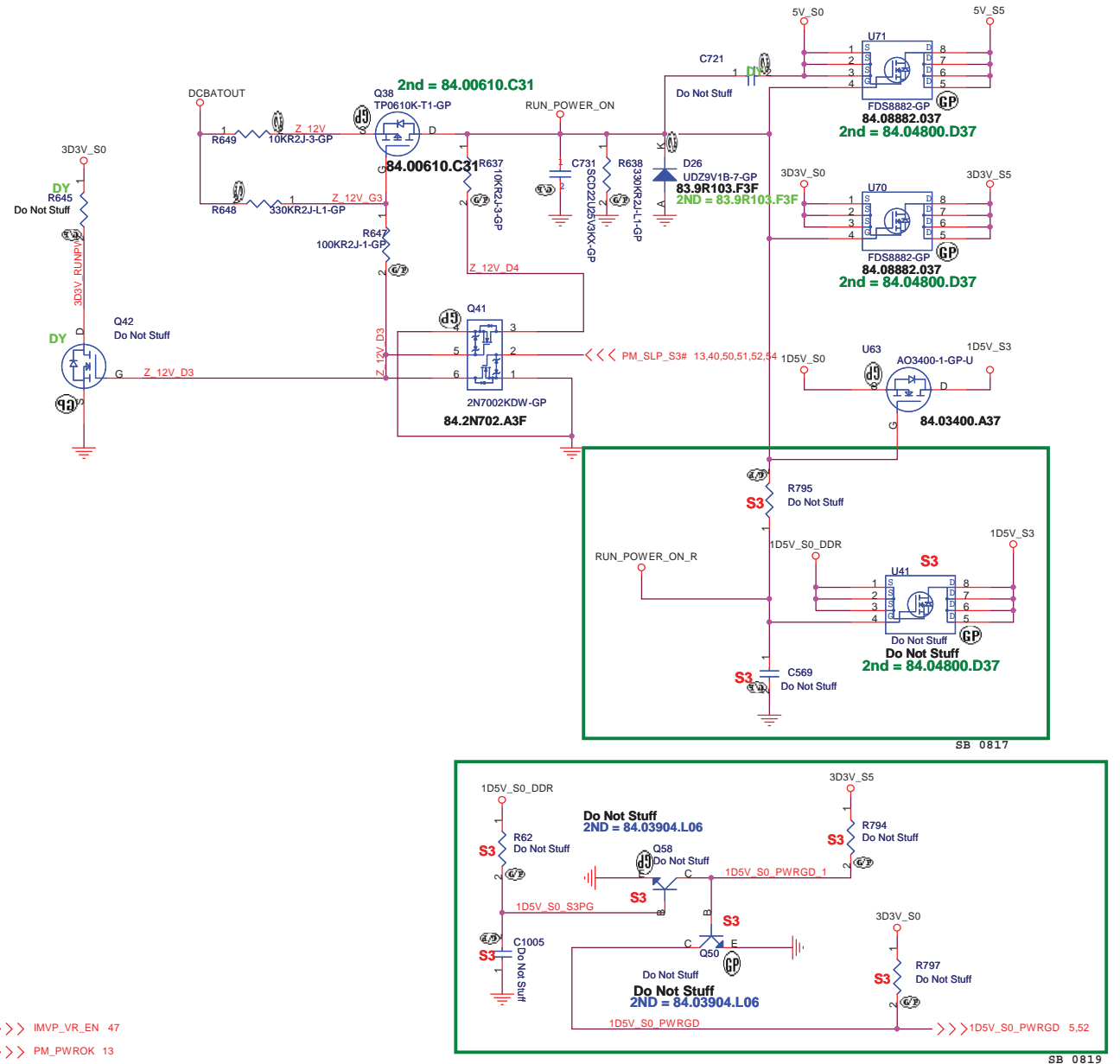
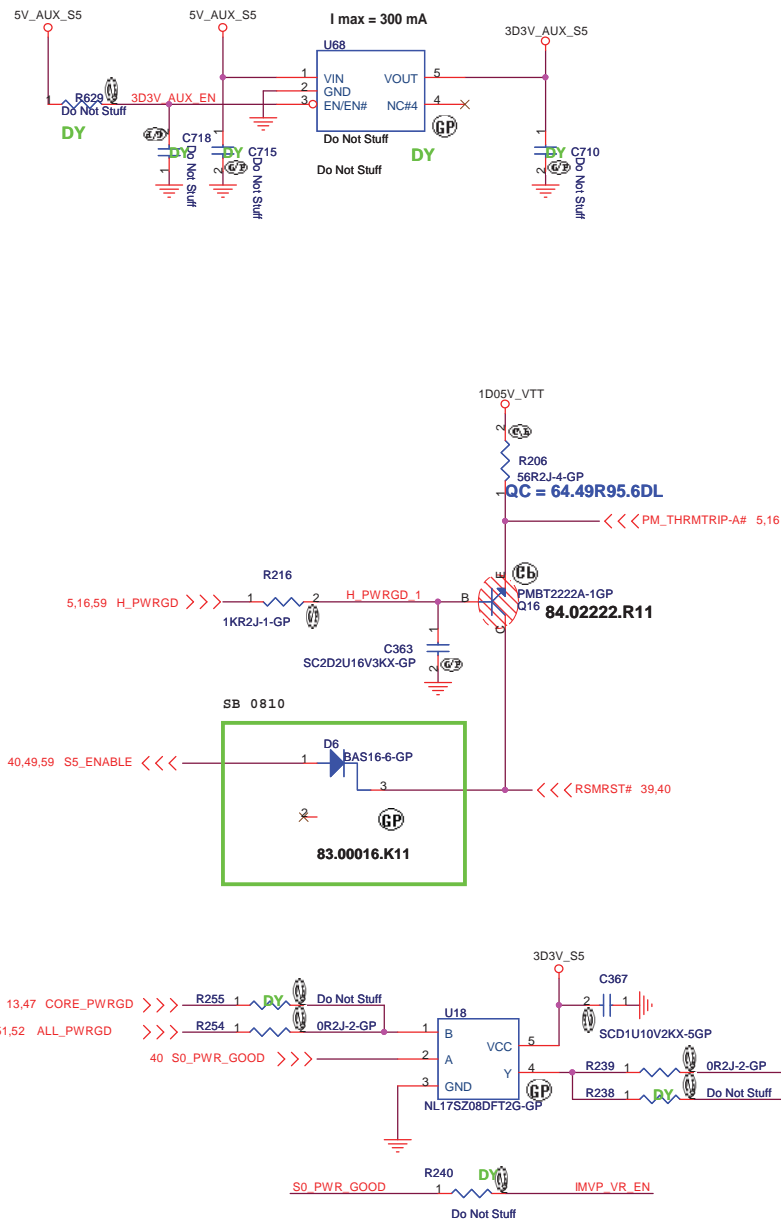
緯創資通 **Wistron Corporation**
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Title			
LED&POWERBD CONN			
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Run Power

Aux Power

3D3V_AUX_S5



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Title

RUN POWER and 3D3V AUX S5

Size

Document Number

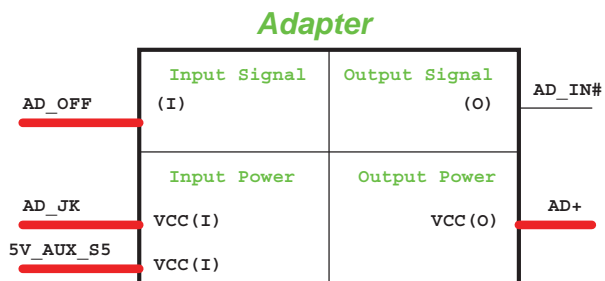
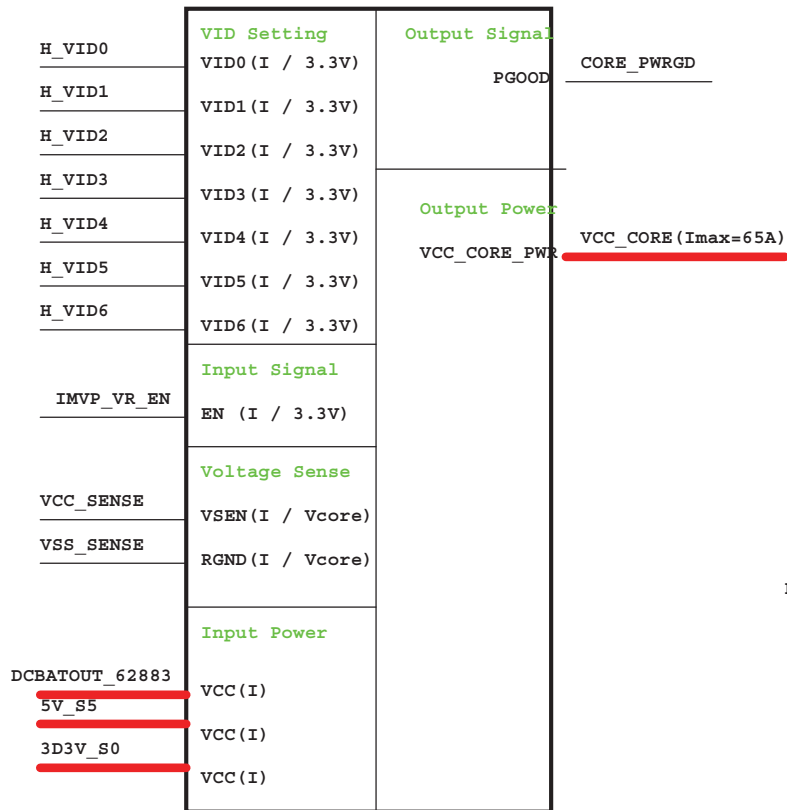
JV50-CP

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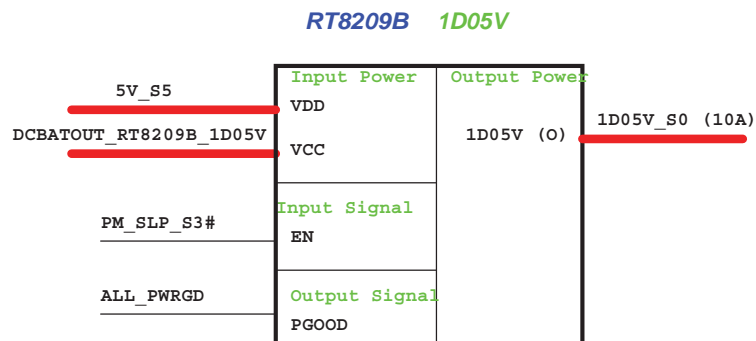
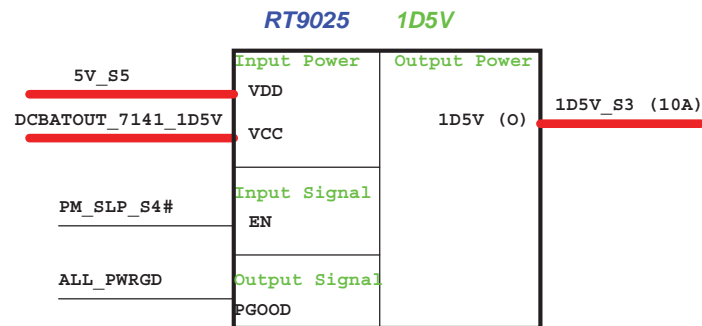
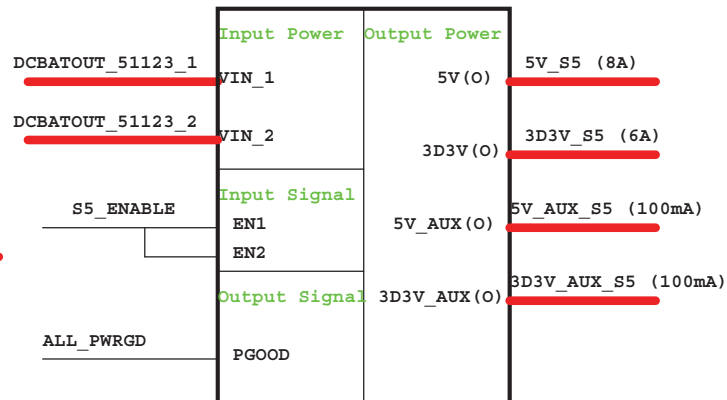
Date: Thursday, September 03, 2009

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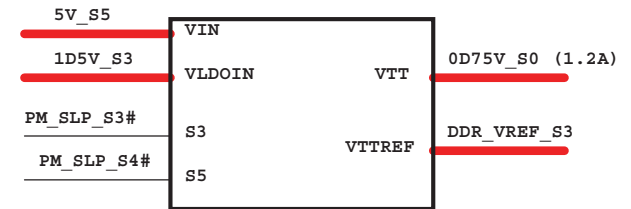
ISL62883 VCC_CORE



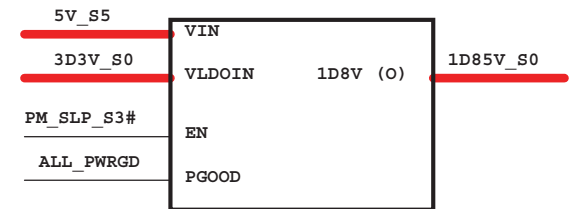
TPS51123 5V/3D3V



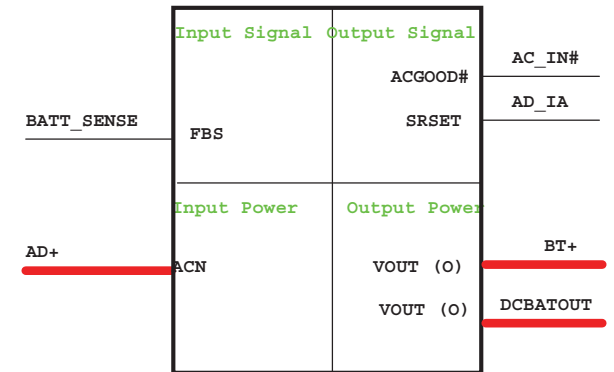
RT9026 0D75V_S0



RT9025 1D8V



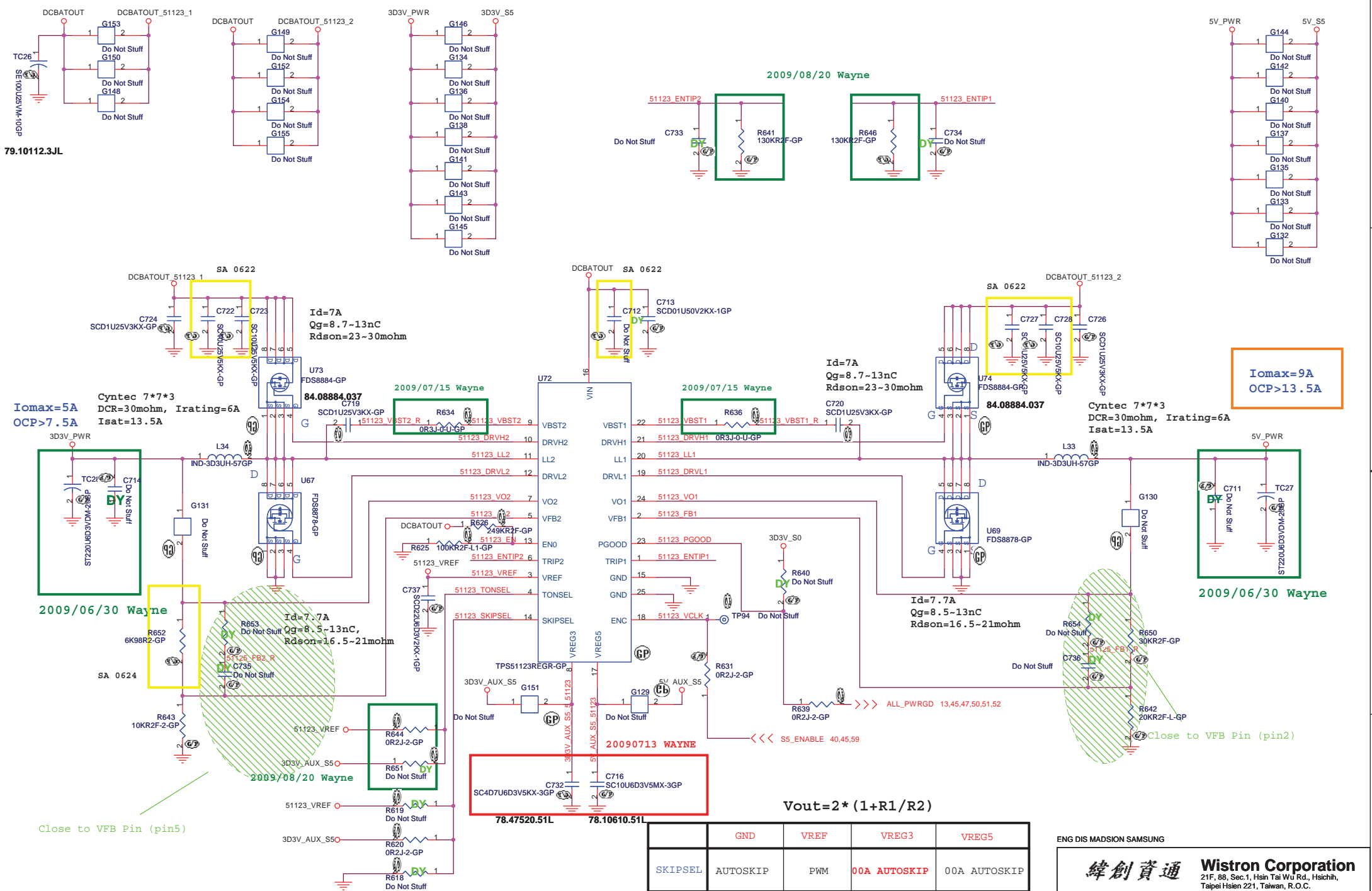
Charger BQ24745



ENG DIS MADISON SAMSUNG

緯創資通 Wistron Corporation
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Power Block Diagram		
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	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation

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Title

TPS51123 5V/3D3V

Size

Document Number

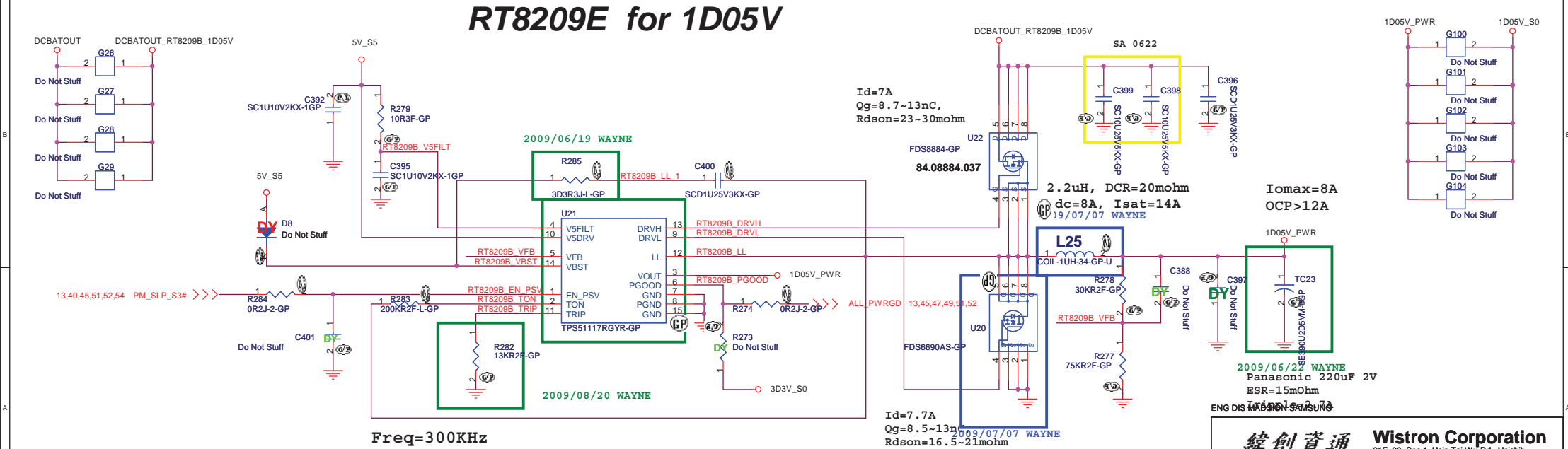
Rev

SA

Date: Thursday, September 03, 2009

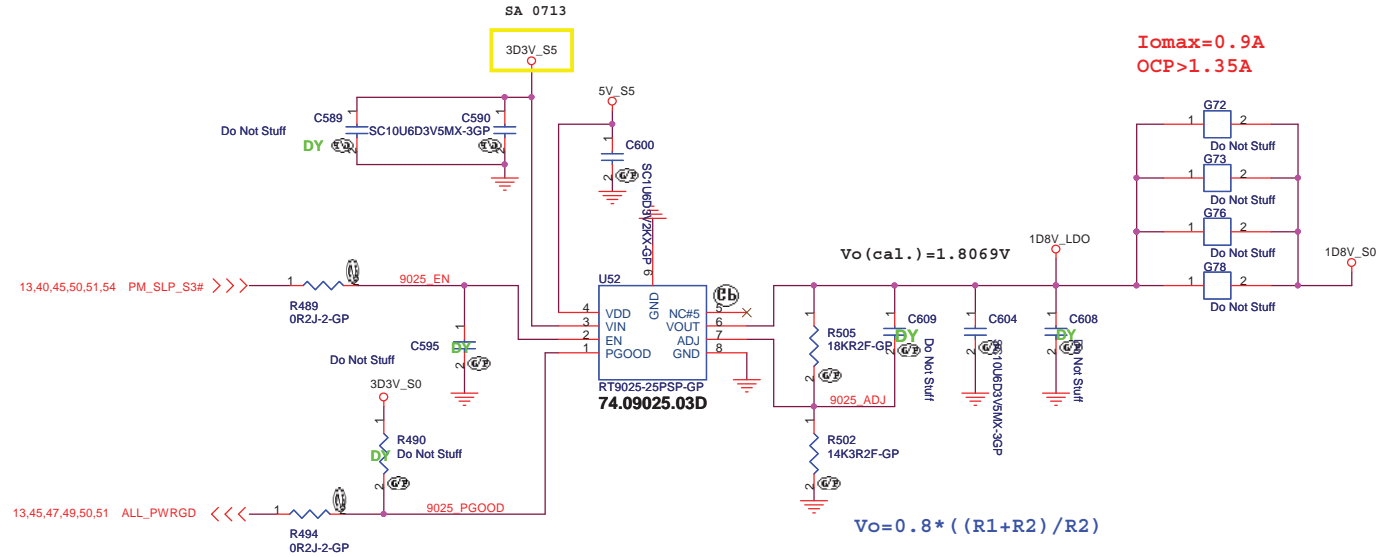
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RT8209E for 1D05V

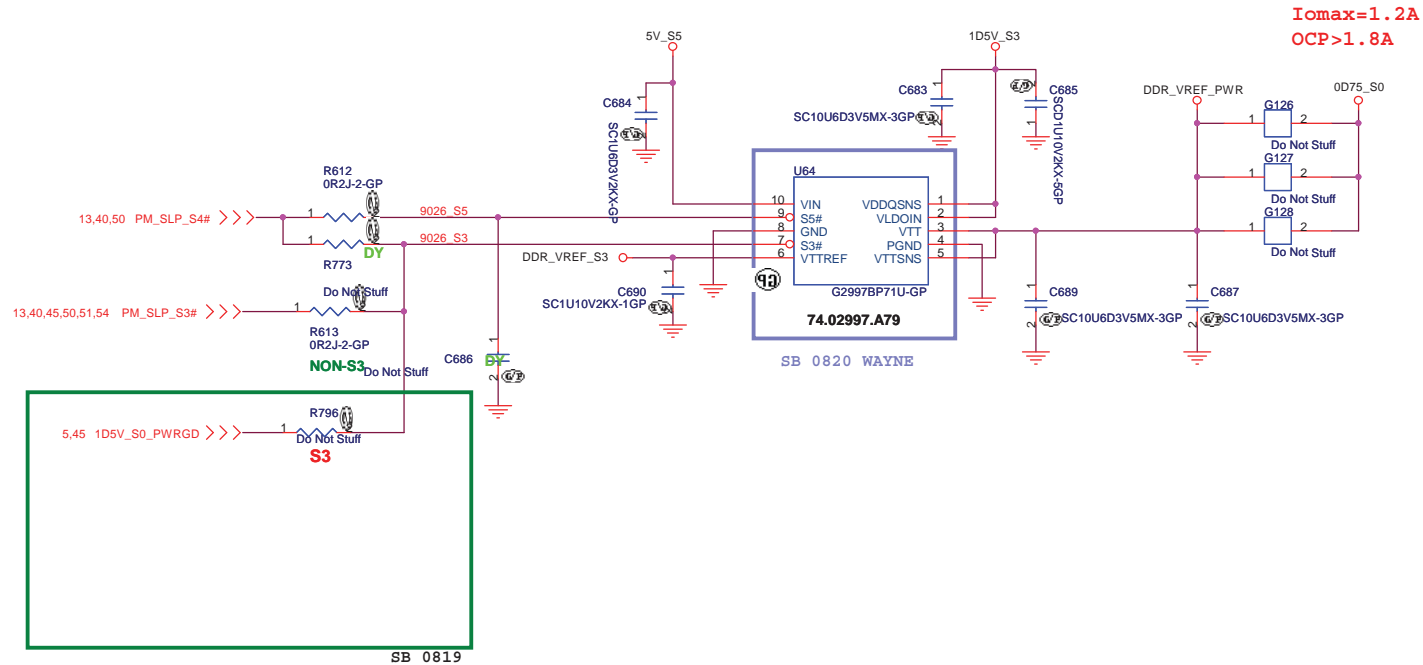


Title			
APW7141 1D5V / RT8209B 1D05V			
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RT9025 for 1D8V_S0



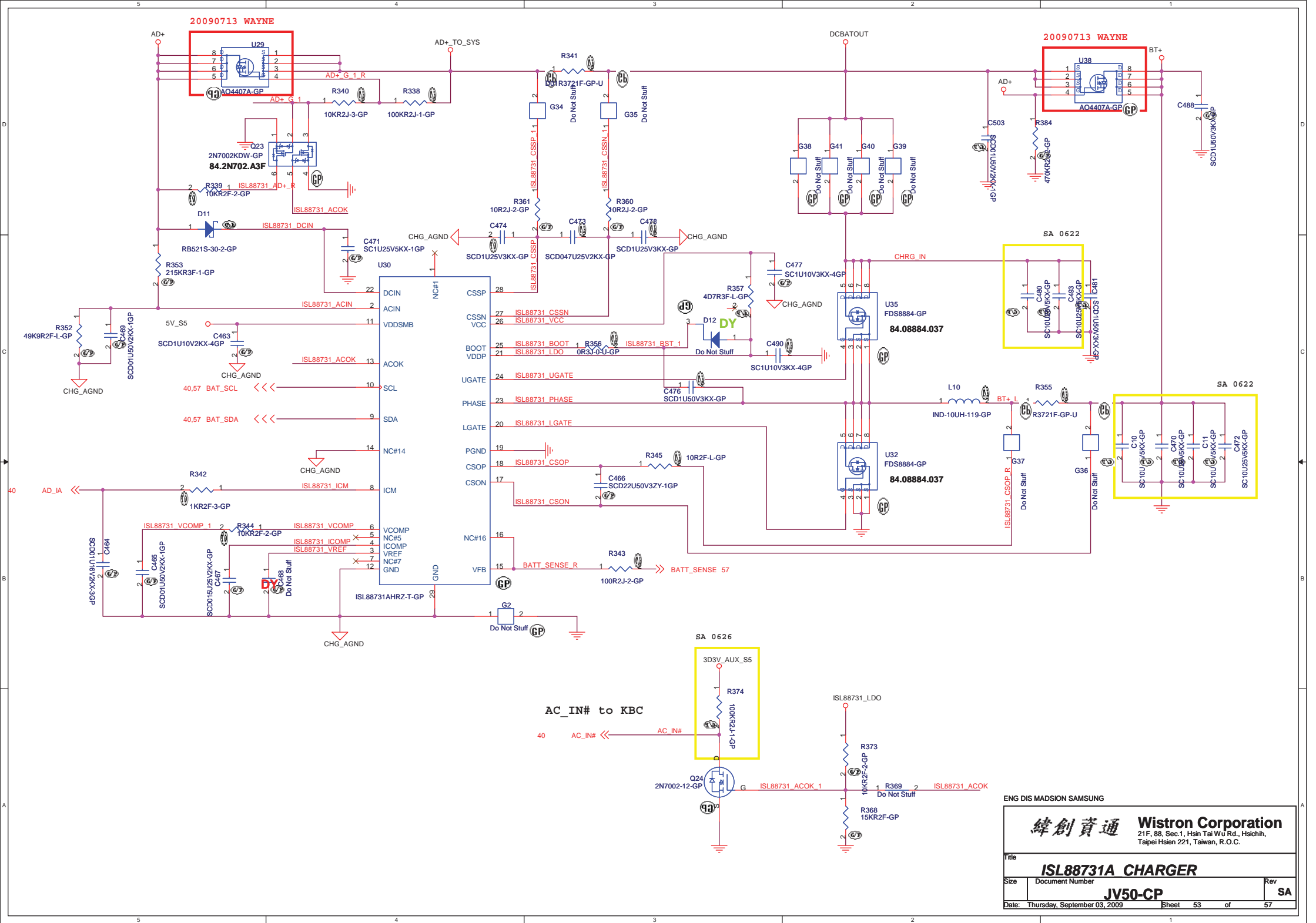
RT9026 for 0D75V_S3

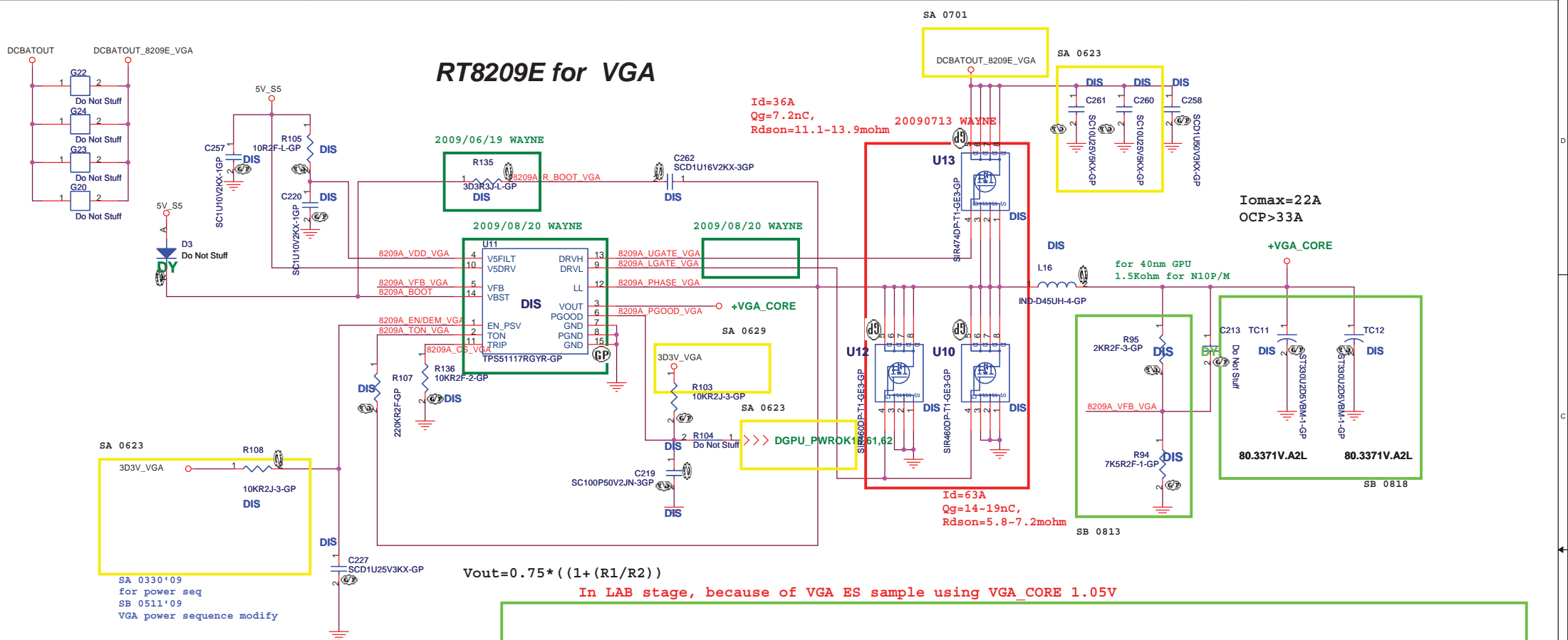


ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

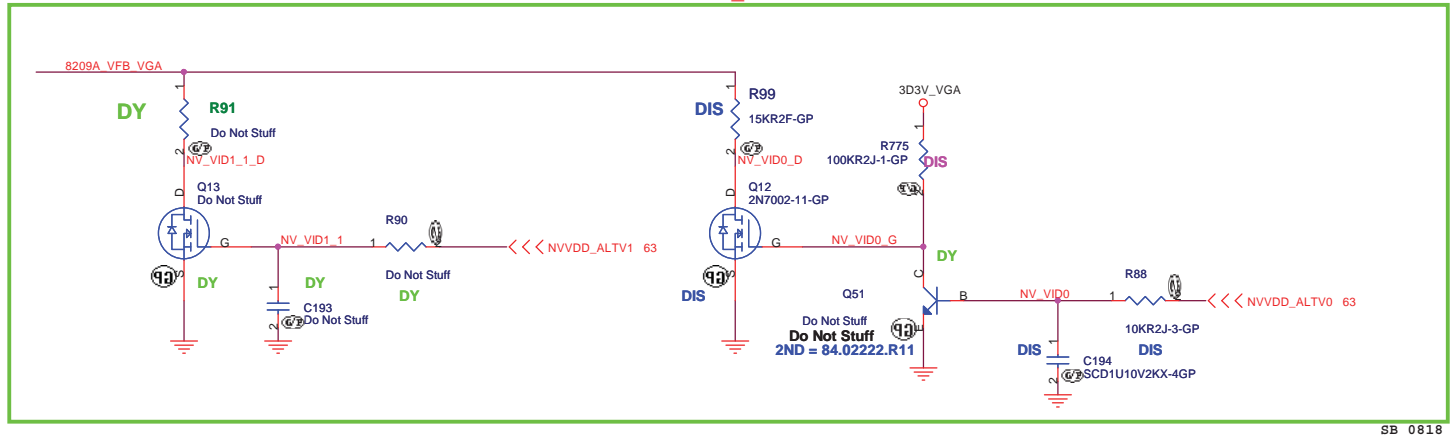
Title		Rev	
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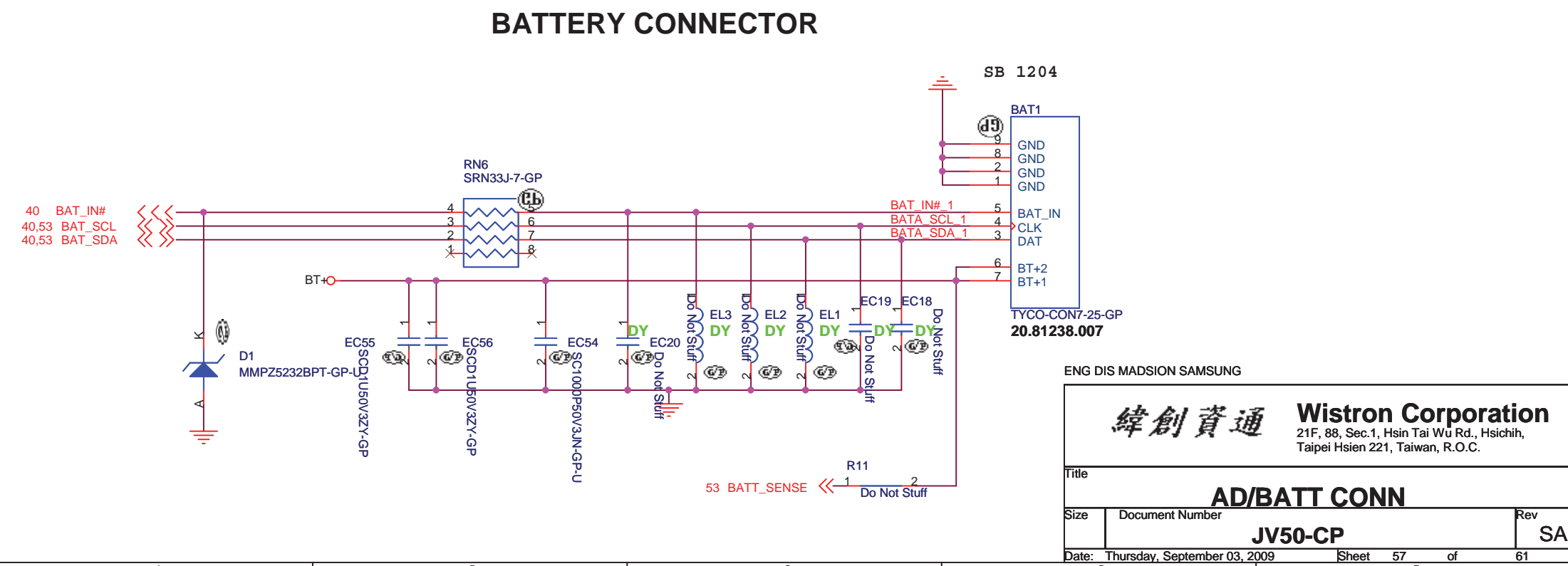
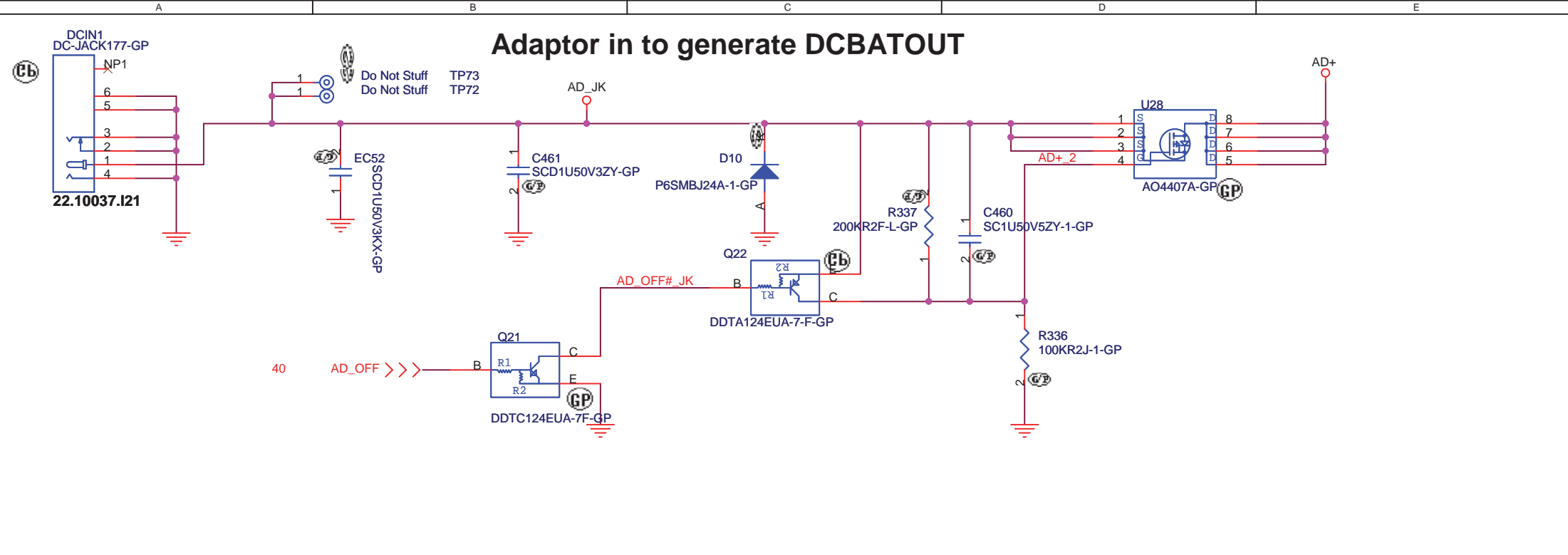


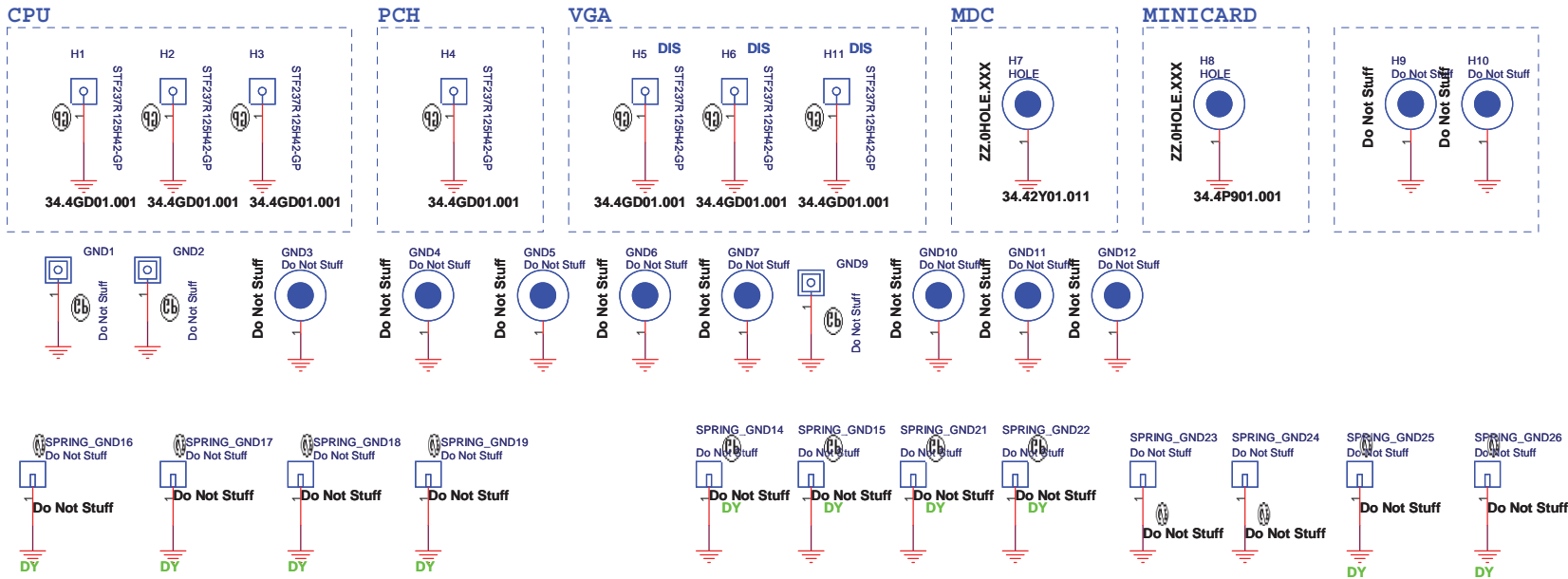
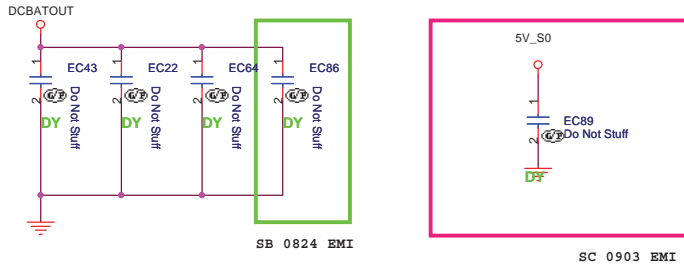
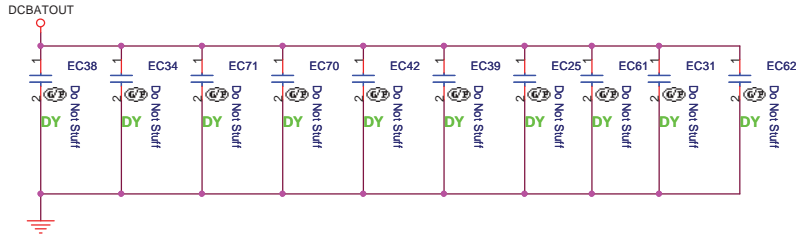
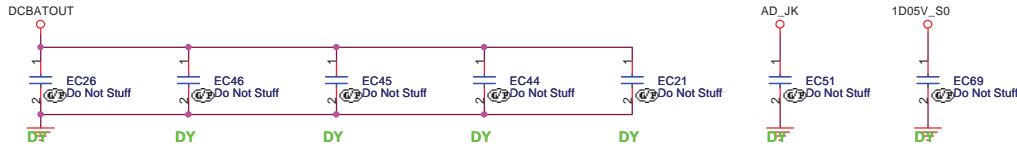
$$V_{out} = 0.75 * ((1 + (R1/R2)))$$

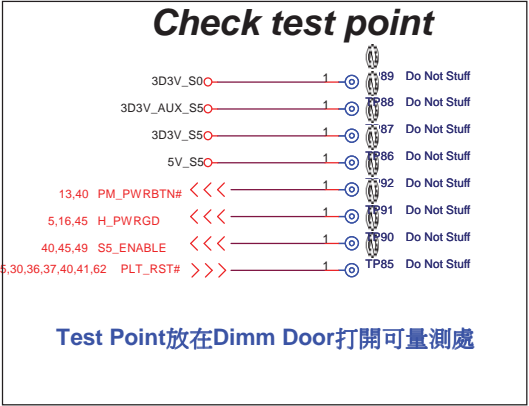
In LAB stage, because of VGA ES sample using VGA_CORE 1.05V



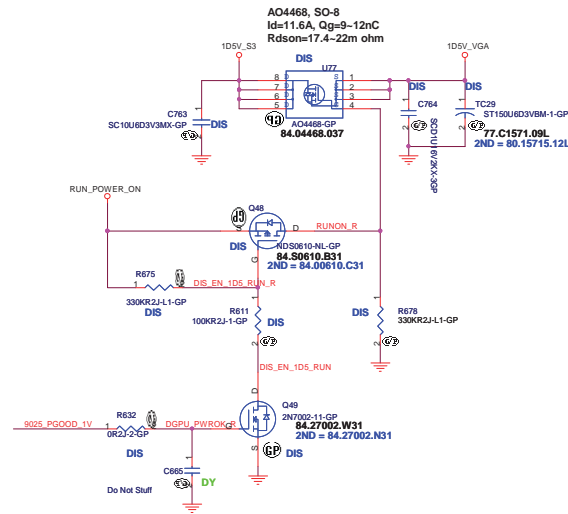
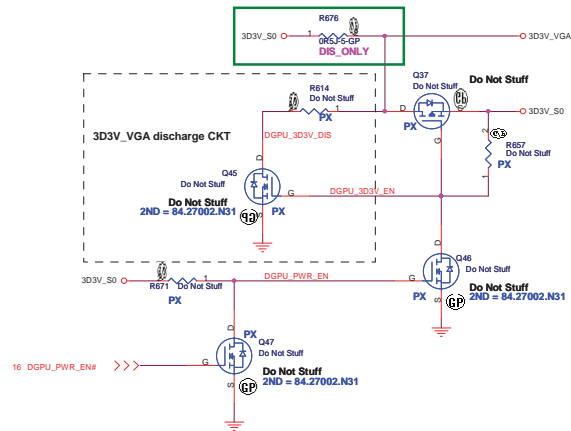
	I/O	Inter Pull Low	GPIO TABLE
NVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.95V



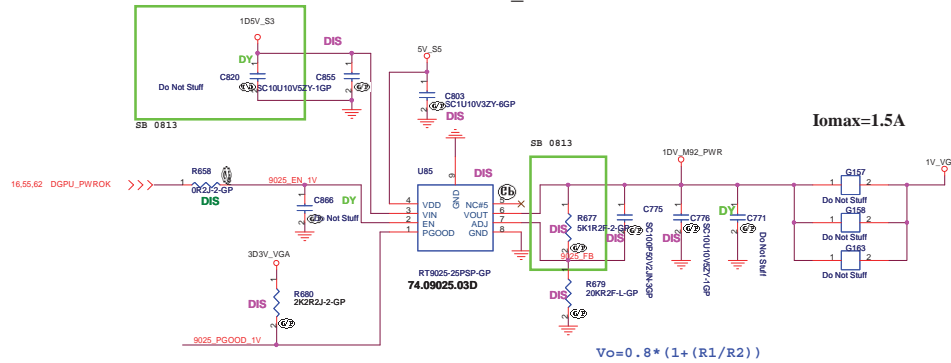




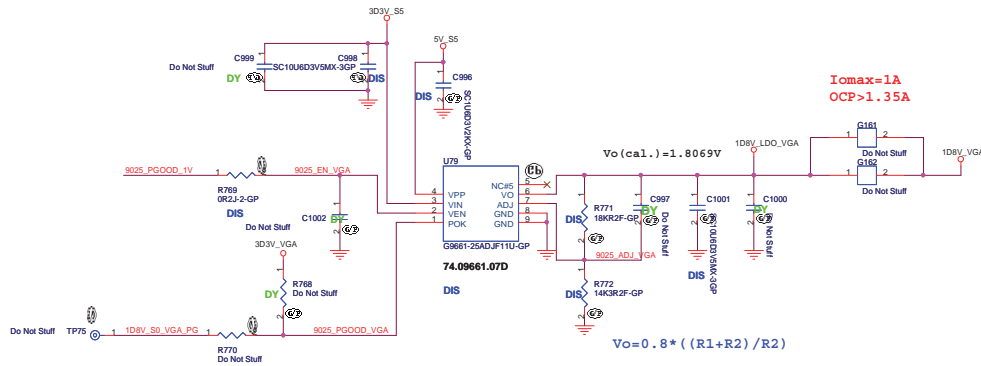
+3VS to 3.3V_DELAY Transfer



RT9025 for 1V_VGA

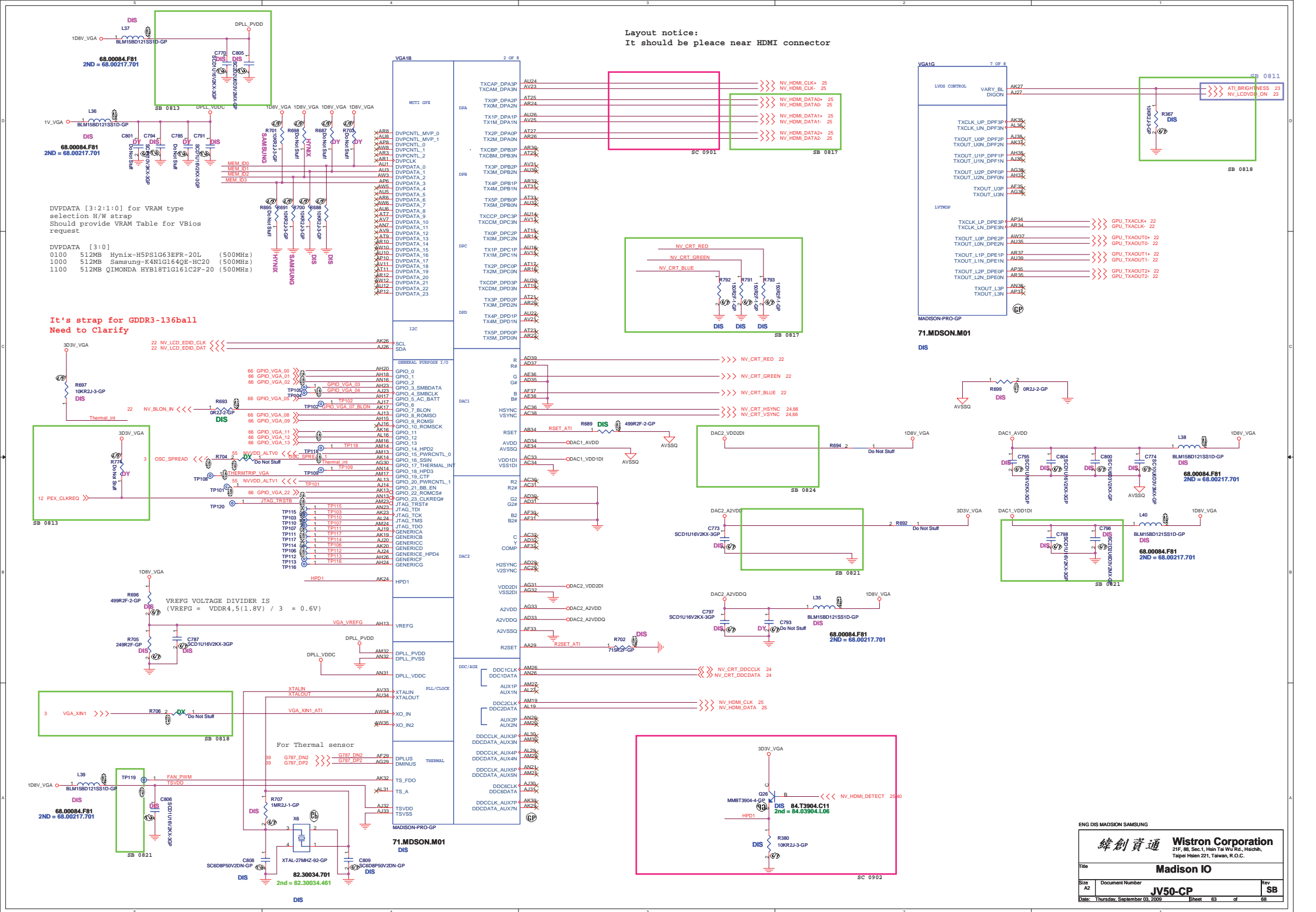


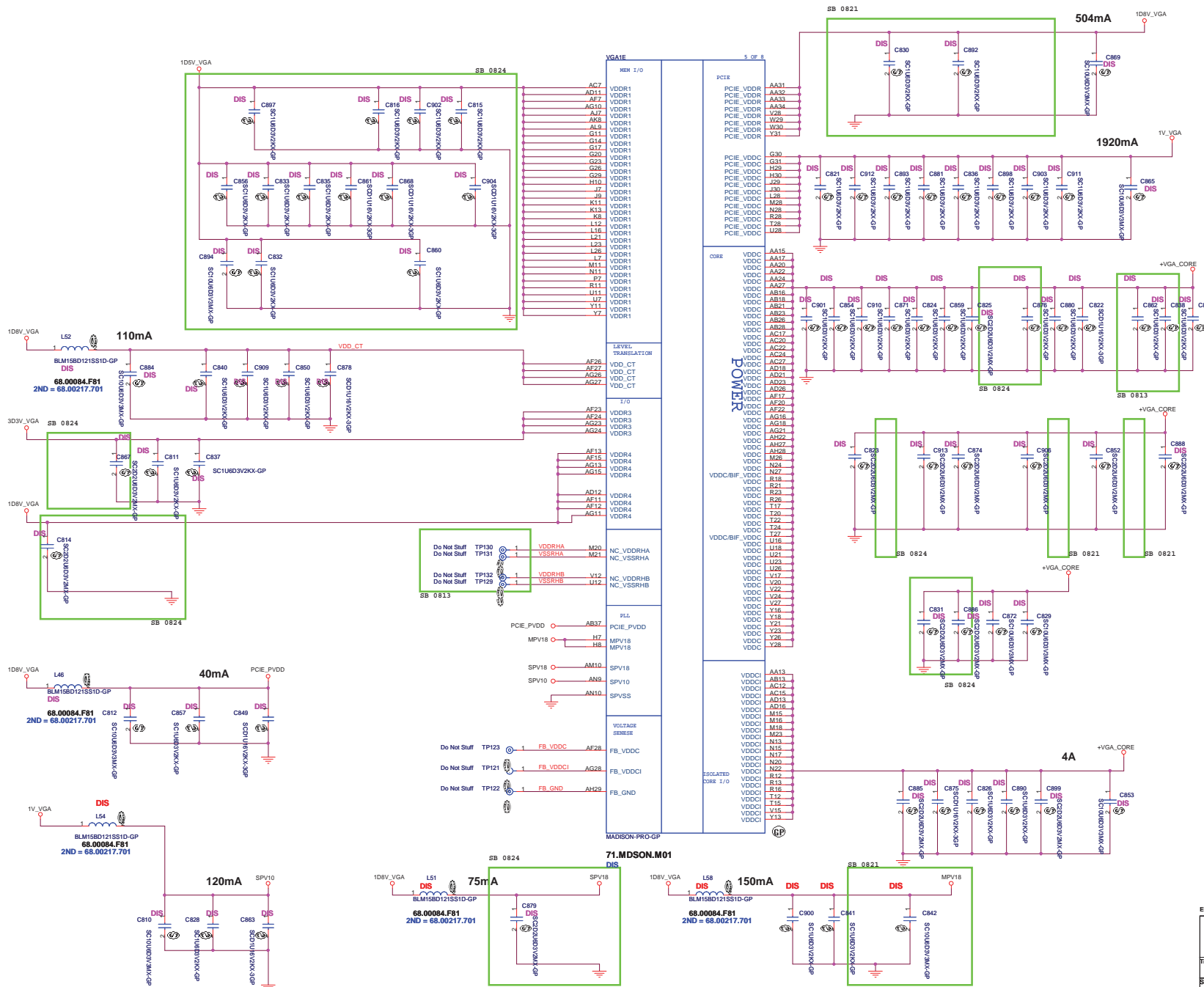
G9661 for 1D8V_VGA

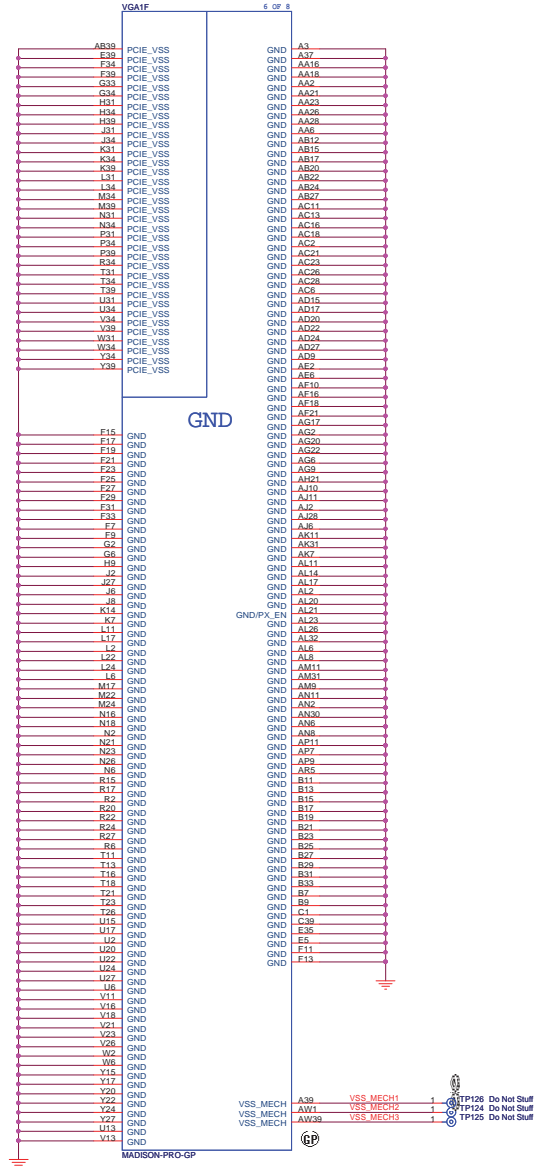
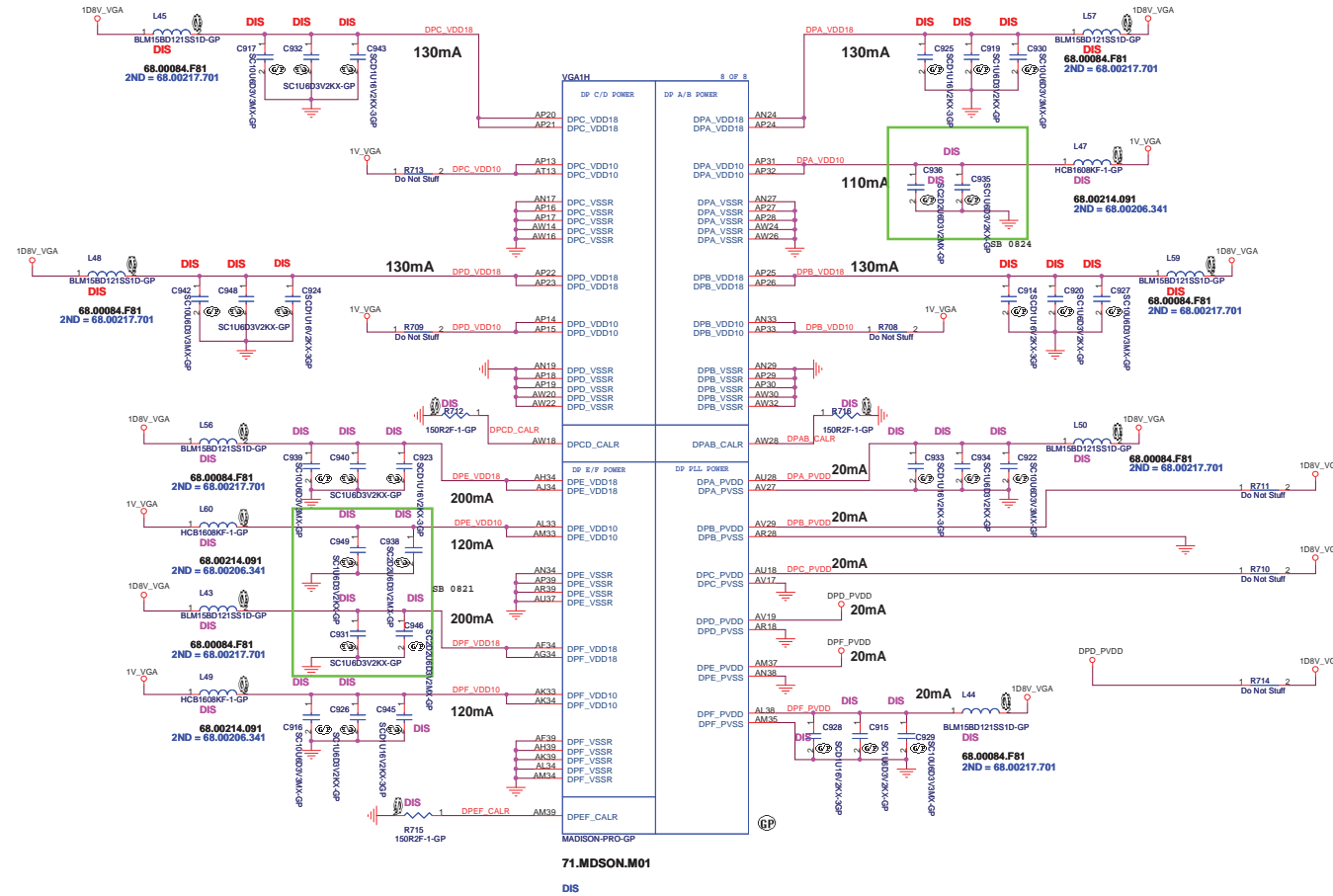


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Layout notice:
It should be place near HDMI connector

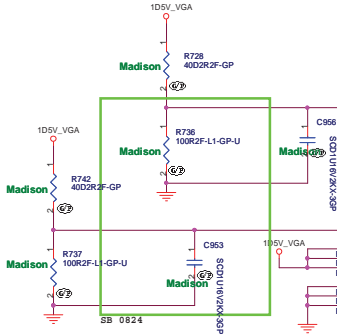






For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVREF	1.5V	1.8/1.5V	1.5V
MVREF TO PWR	40.2R	40.2R	40.2R
MVREF TO GND	100R	100R	100R



Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

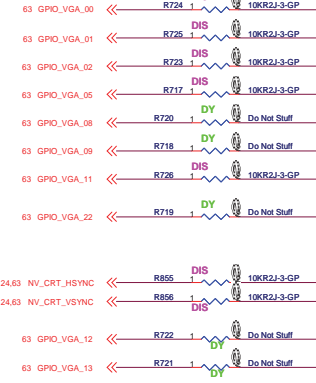
MADISON-PRO-GP

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS
TX_PWRS_ENB (Internal PD)	GPIO0	PCIe Full Tx Output Swing Transmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	x
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	x
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1, then Config[3:0] defines the ROM type if BIOS_ROM_EN=0, then Config[3:0] defines the primary memory aperture size	x x x
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI	x x

DIS

AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET			
H2SYNC, GENERICC, GPIO2, GPIO1			

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A
256MB	x001	Microelectronics	M25P10A
64MB	x010		M25P20
32MB	x		M25P40
512MB	x		M25P80
1GB	x	Chingis (formerly PMC)	Pm25LV512A
2GB	x		Pm25LV010A
4GB	x		



71.MDSON.M01

Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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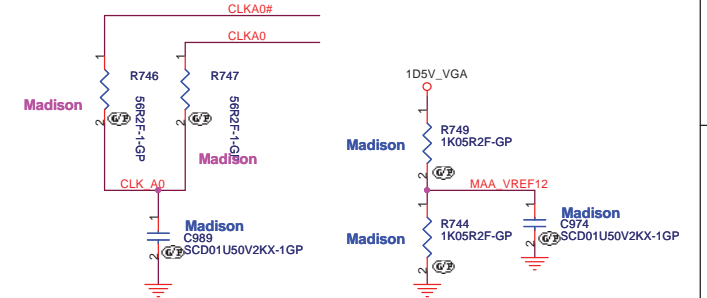
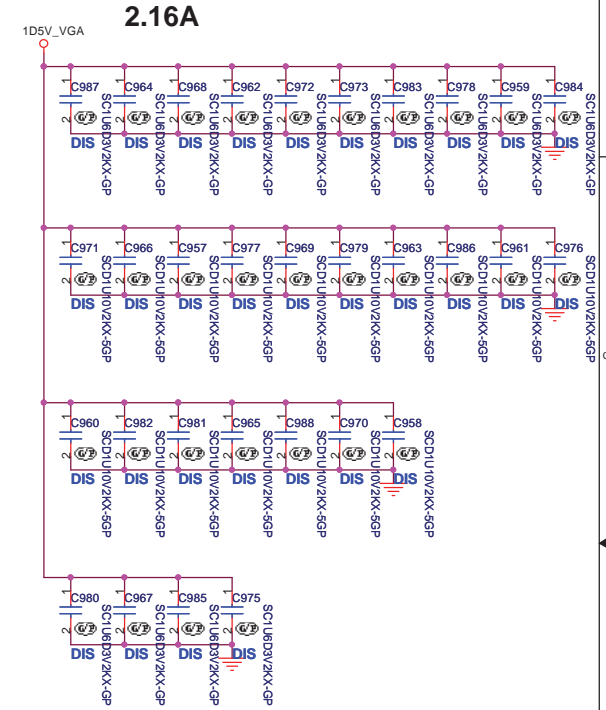
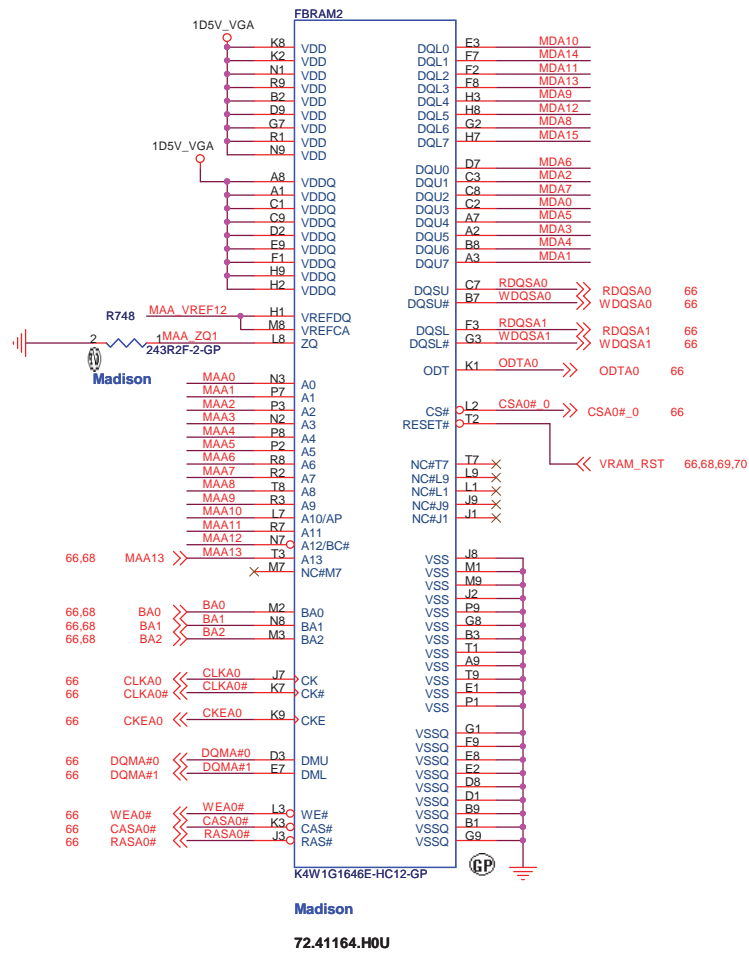
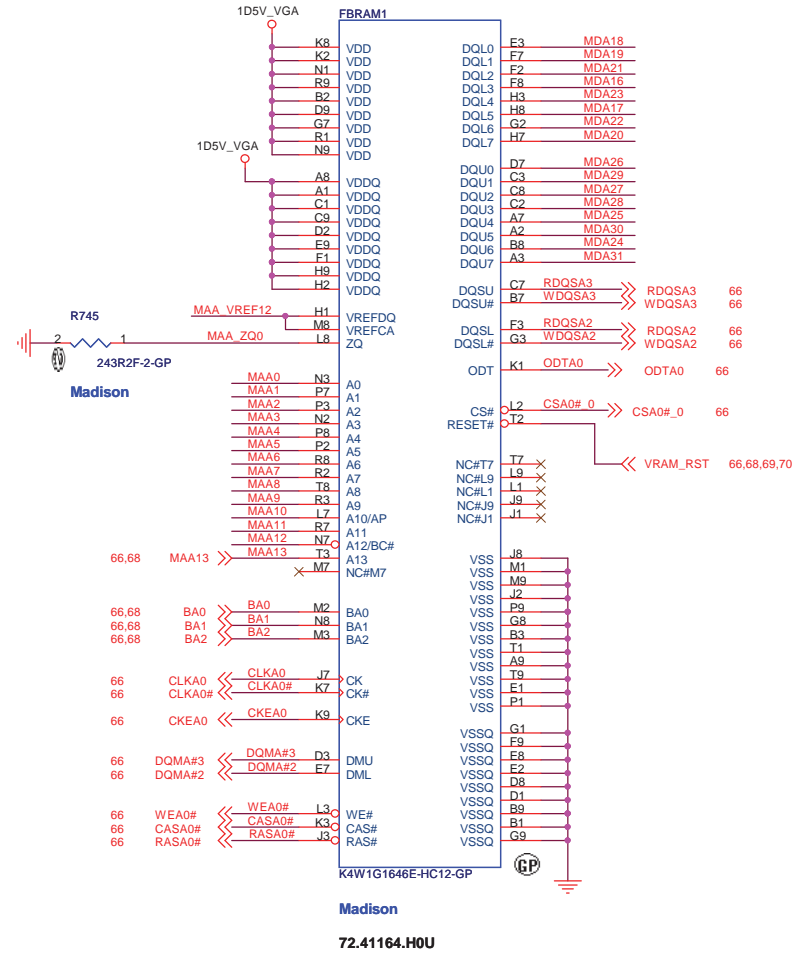
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Taipei Hsin 221, Taiwan, R.O.C.

Rev SB

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Title			
VRAM(1/4)			
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HYNIX: 72.51G63.C0U

66,68 DQMA#[0..7] <<>

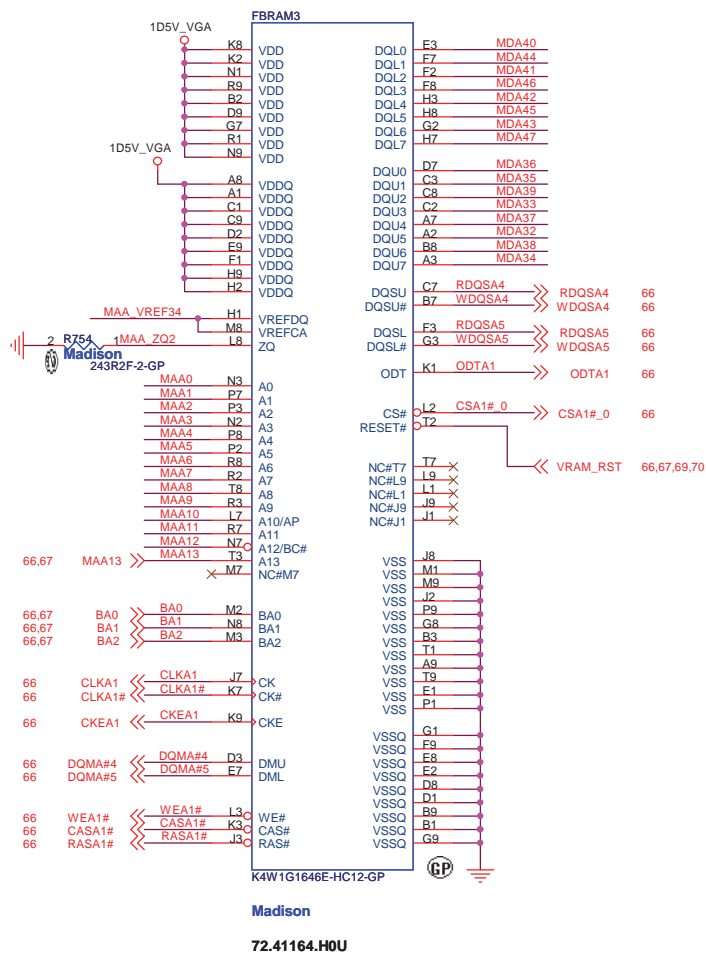
66,68 RDQSA#[0..7] <<>

66,68 WDQSA#[0..7] <<>

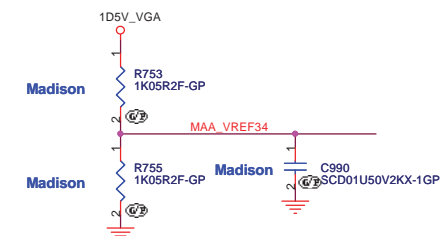
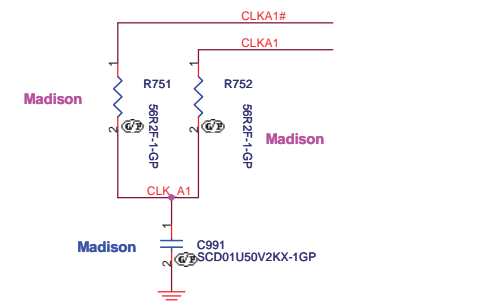
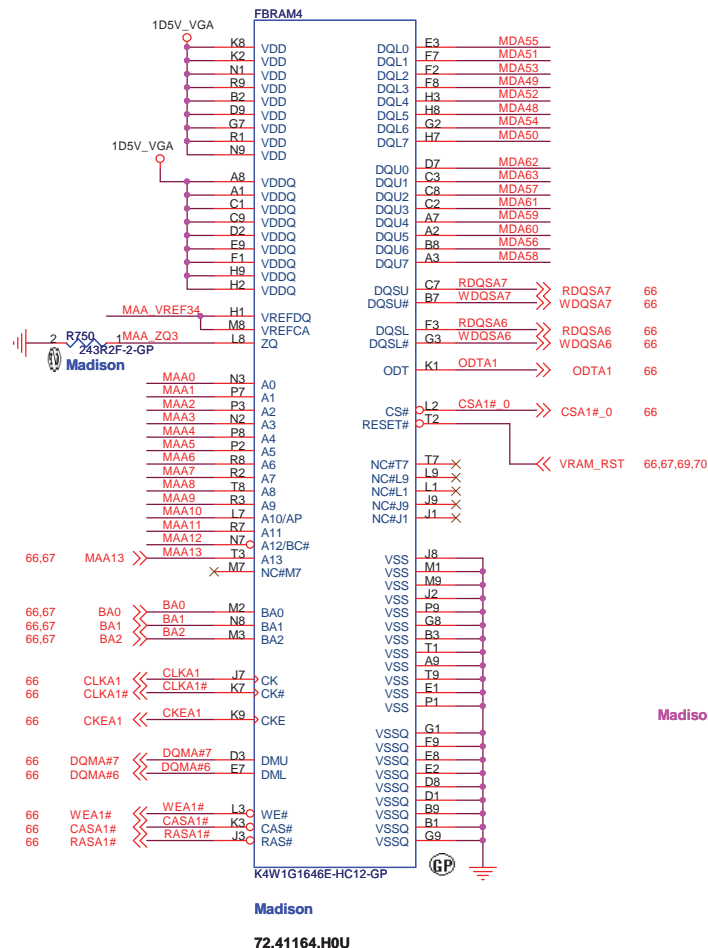
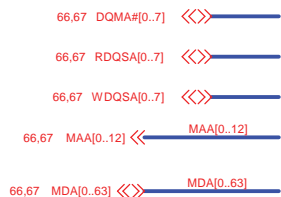
66,68 MAA[0..12] <<>

66,68 MDA[0..63] <<>

DDR3



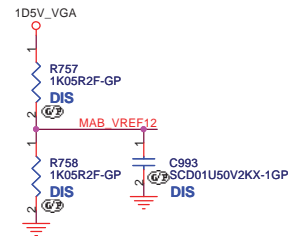
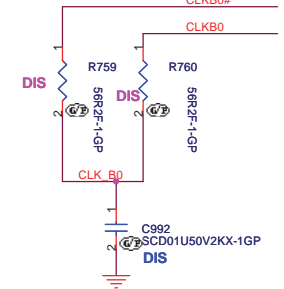
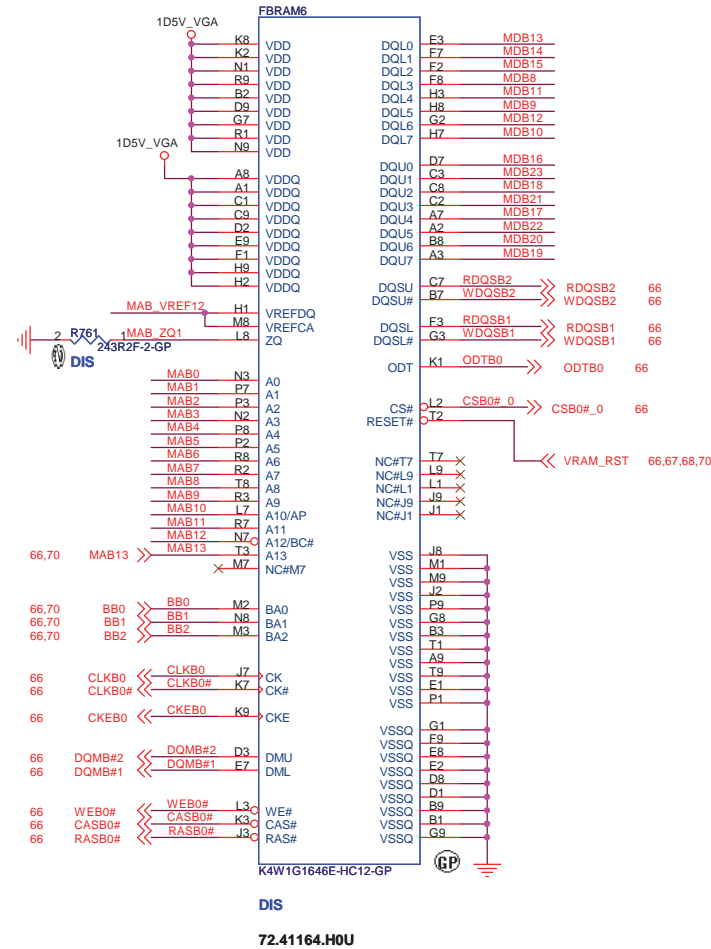
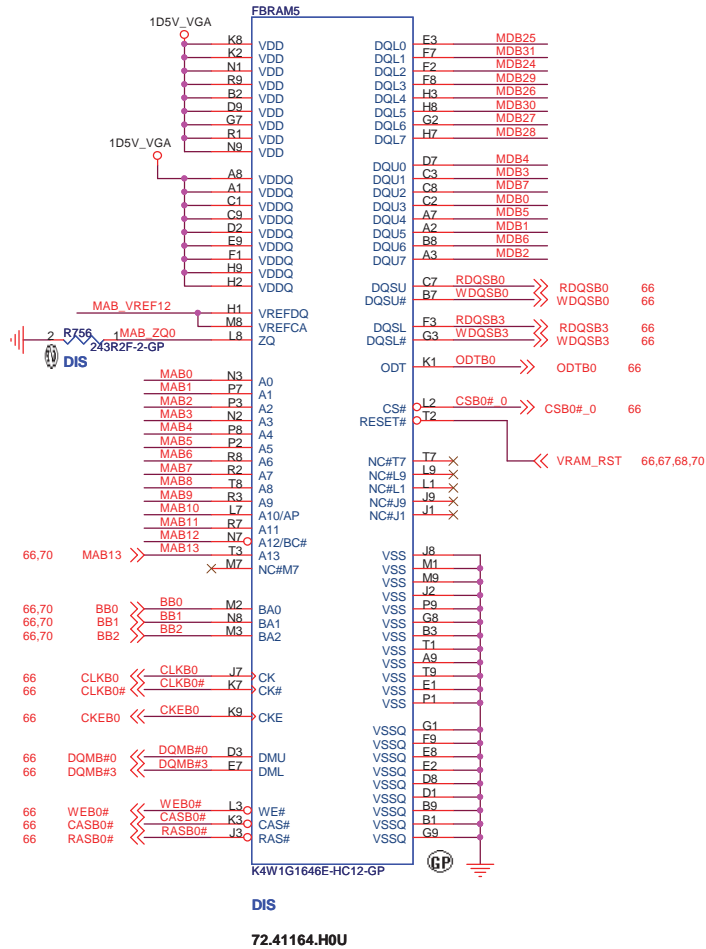
SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



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HYNIX: 72.51G63.C0U

66,70 DQMB[0..7] <<>>

66,70 RDQSB[0..7] <<>>

66,70 WDQSB[0..7] <<>>

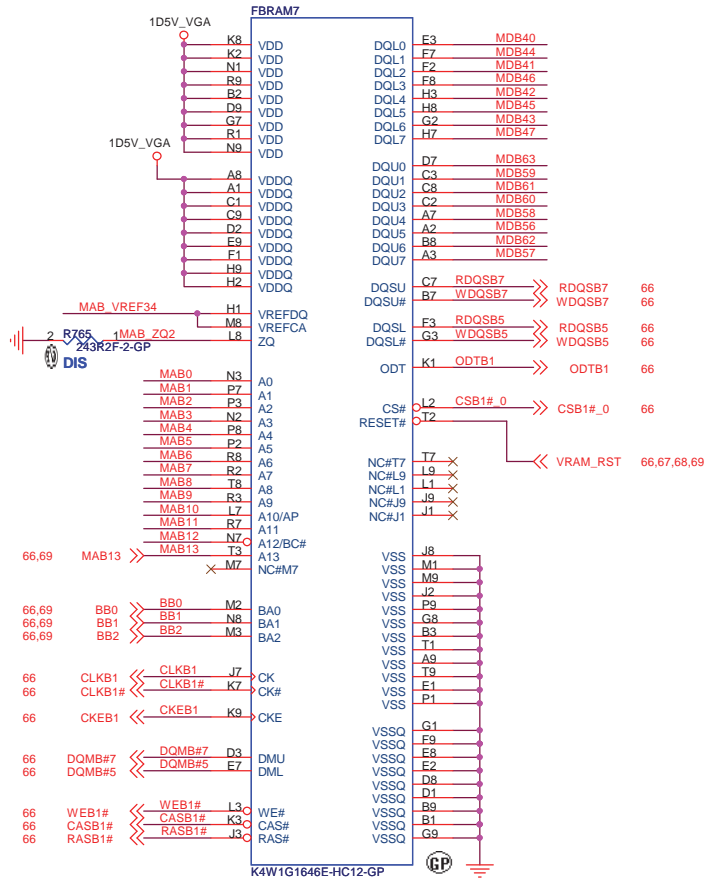
66,70 MAB[0..12] <<>>

66,70 MDB[0..63] <<>>

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SAMSUNG: 72.41164.H0U

HYNIX: 72.51G63.C0U

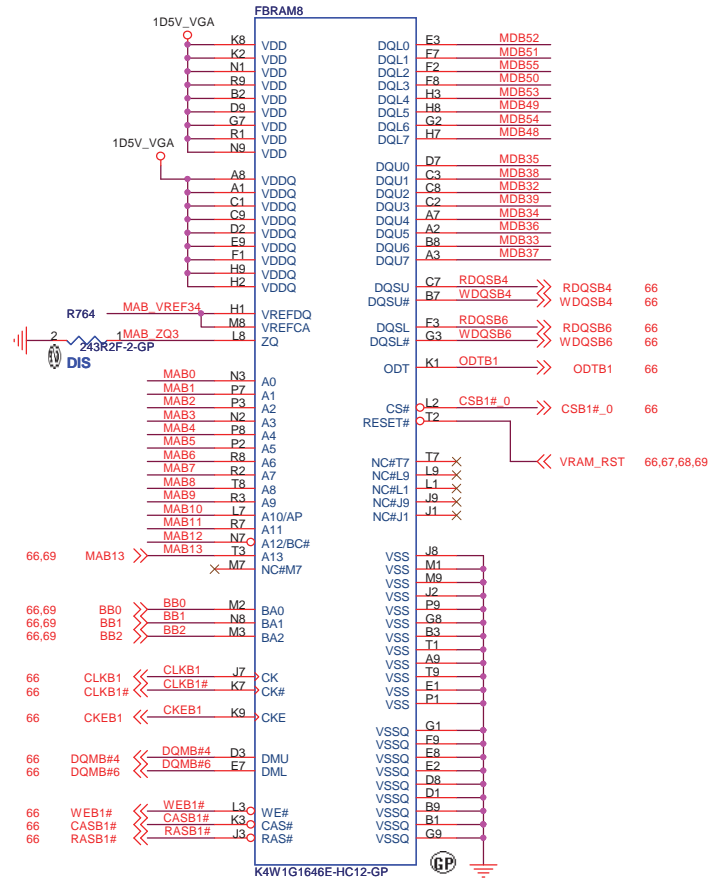
66,69 DQMB[0..7] <<>

66,69 RDQS[0..7] <<>

66,69 WDQS[0..7] <<>

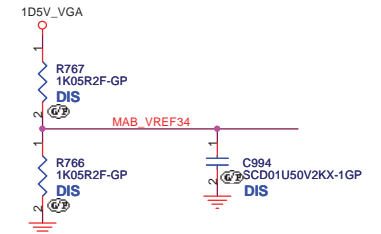
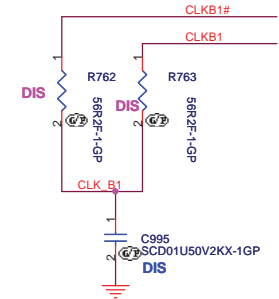
66,69 MAB[0..12] <<>

66,69 MDB[0..63] <<>



DIS

72.41164.H0U



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Title			
Modify History			
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